DESIGN OF CMOS BASED CONFIGURABLE ANALOG BLOCK FOR FIELD PROGRAMMABLE ANALOG ARRAY

BY

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To

My honorable mother & father

My dear brothers & sisters

and

My lovely wife & daughter

Thanks for believing in me and for your unconditional support

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All praise and thanks is due to almighty Allah, the lord of the worlds who provides me with the courage and patience to complete this work.

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LIST OF ABBREVIATIONS

APF : All Pass Filter

A/S : Adder Subtractor

BJT : Bipolar Junction Transistor

BPF : Band Pass Filter

BW : Bandwidth

CAB : Configurable Analog Block

CAC : Configurable Analog Cell

CCII : Second Generation Current Conveyor

CFOA : Current Feedback Operational Amplifier

CMOS: Complementary Metal Oxide Semiconductor

CT : Continuous Time

DAC : Digital to Analog Converter

DC : Direct Current

DT : Discrete Time

EPAC : Electronically Programmable Analog Circuit

FG : Floating Gate

FPAA : Field Programmable Analog Array

FPGA : Field Programmable Gate Array

HPF : High Pass Filter

INT : Integrator

IC : Integrated Circuit

LPF : Low Pass Filter

M/D : Multiplier Divider

MITE : Multi Input Transistor Element

MOSET : Metal Oxide Semiconductor Field Effect Transistor

Op-Amp: Operational Amplifier

OTA : Operational Transconductance Amplifier

PCAP : Programmable Capacitor

PCM : Programmable Current Mirror

PCS : Programmable Current Source

PD : Phase Detector

PL : Programmable Logic

PLL : Phase Locked Loop

PR : Programmable Register

RASP : Reconfigurable Analog Signal Processing

RTC : Reconfigurable Translinear Cell

S**M** : Switch Matrix

SC : Switched Capacitor

THD : Total Harmonic Distortion

TLE : Translinear Element

TLP : Translinear Principle

TRAC : Totally Reconfigurable Analog Cell

ABSTRACT

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In this thesis, a new current mode configurable analog block (CAB) for field programmable analog array (FPAA) based on transistor level design has been proposed. The design adopts MOSFETs operating in saturation region. Three functional cells capable of performing addition, subtraction integration, multiplication, division and pass have been reported. The programming and tuning of the CAB is achieved by digitally modifying bias condition and some switches. In order to test the validity of the proposed CAB, it has been used to realize four different applications: a universal second order filter, a fourth order band pass filter, a modulation-demodulation system and a phase detector. Simulation was carried out using Tanner EDA Tools in $0.35\mu m$ standard CMOS technology. The results confirm strong agreement between theory and simulation with the main attractive features of simplicity, low power consumption and high bandwidth operation.

ملخص الرسالة

الاسم الكامل: أمين سالم عوض بن عبادي

عنوان الرسالة: تصميم دوائر وحدات تماثلية قابلة للتشكل لحقول المنظومات التماثلية المبرمجة باستخدام تقنية (MOSFET)

التخصص: الهندسة الكهربائية

تاريخ الدرجة العلمية: سبتمبر 2014 م

في هذه الأطروحة تم عرض تصميم دوائر لوحدات تماثلية قابلة للتشكل لحقول المنظومات التماثلية المبرمجة باستخدام نمط التيار للترانزستورات في منطقة التشبع. لهذا الهدف تم عرض ثلاث خلايا قادرة على تنفيذ عمليات : الجمع والطرح والتكامل والضرب والقسمة والعبور. تتم عملة البرمجة والضبط باستخدام التعديل الرقمي لشروط تهيئة هذه الوحدات بالإضافة لبعض المفاتيح. لإختبار صحة عمل التصميم المقترح تم استخدامه في بناء تطبقات مختلفة مثل مرشح الدرجة الثانية العام و مرشح امرار الحزمة الرباعي و نظام التضمين وإزالة التضمين وكذالك نظام كاشف الطور. تمت المحاكاة باستخدام برنامج (تانر) وتم الحصول على نتائج متوافقة مع التحليل النظري . أهم الميزات التي يتحلى بها هذا التصميم هي البساطة وقلة استهلاك الطاقة بالاضافة الى العمل في عرض نطاق ترددي عالي.

CHAPTER 1

INTRODUCTION

One of the biggest breakthroughs in the field of digital integrated circuits has been the field-programmable gate array (FPGA). Since the early 90s of the past century, researchers started to develop many designs of the analog counterpart of FPGA which is "Field Programmable Analog Array", FPAA. This has led to several improvements in this area. However, while field-programmable analog arrays (FPAAs) researchers are attempting to fill a similar void in the analog field as in the digital, they have not been able to develop a design to a point where it is being adopted by designers [1].

1.1 Analog Circuits

Natural signals exist in the nature in analog form. To process natural signals, sensors are used to capture the variation in the signal and analog circuits are used to interpret the natural signal and convert it into an electrical signal which can be processed. In general much of the processing of signals is done in the digital domain; however, many signals require some analog processing before converting them into digital signals and processing them with a digital signal processor [2].

Even though, digital processing circuits are dominating the market, analog solutions are becoming increasingly competitive with digital circuits especially for dense, low-power,

high-speed applications [3]. This is because analog circuits can perform important signal processing functions faster, using less power, and on less silicon area than their digital counterparts.

However, Analog design is more complex and has many trades-off and issues to be considered. One of the reasons analog design is so much more complex than digital is that the number of design options and trades-off it involves is much larger than in the digital domain. Also, analog designers have significantly less freedom in ignoring low-level circuit interaction of high-level blocks in a hierarchical design. A carefully designed multi-function analog circuit such as an FPAA can successfully address these issues, delivering the full potential of analog circuits to a designer, who may or may not be an analog expert [4].

Analog circuits are rather unlikely to be eliminated entirely from the electronic design, nor to be reduced to some simple, residual form in a predominantly digital design world. Therefore, it is of utmost importance to ease the analog design process. This can be done if the improvements in the FPAA's design reach a level where the FPAA can be adopted by designers to be utilized for most of their designs.

1.2 Motivation

Several improvements in the area of CAB & FPAA design have been achieved over the years. However, while field-programmable analog arrays (FPAAs) researchers are attempting to fill a similar void in the analog field as in the digital, they have not been

able to develop a design to a point where it is being adopted by designers. Some FPAAs have been developed commercially however; these FPAAs tend to be limited in their applications [2]. As a result, commercial FPAAs have not had the same success of commercial FPGAs. One of the reasons for this is might be the lack of a universal block from which analog circuits could be systematically built, as gates are to digital circuits [1].

Analog simulations are often inaccurate and problematic compared to their digital counterparts. This is due to the large number of effects that must be simulated. Often it is not known whether a circuit will work until after it has been built. This can lead to increased costs & time consumption in developing multiple versions of chips before a working prototype is made [2].

The real benefit of FPAA design is to be used to prototype, test and develop analog circuits. Its reconfigurable architecture allows for quick, inexpensive prototyping, which in turn would make the FPAA invaluable in the testing and prototyping of analog circuitry design [2]. In addition, FPAAs can open up the use of analog circuits to designers without deep expertise in the field. So, the drive towards shorter design cycles & lower cost for analog integrated circuits has demanded the development of several improvements in the area of FPAA and their CABs [3].

Currently available commercial and academic FPAAs are typically based on CABs involving operational amplifiers, or other similar analog primitives, with few computational elements per chip. The ever-presented demand on high frequency

operation and lower supply voltages is the main requirement that affect the design of the configurable analog blocks (CABs) of any FPAA [5].

There are many publications in the literature which use active elements such as Op-amp, OTA, CCII or CFOA in the design of CAB [6- 10]. Since these designs are based on the mentioned active elements, the resulting CAB will be limited in performance to the capability of the used elements. Additionally, other designs do not include active elements; rather they are transistor level based designs [1, 5, 11-14]. The transistor level design CAB can be done using MOSFET sub-threshold as in [11], BJT transistors as in [5] or multi trans-linear element (MITE) and floating gate transistors (FG) as in [1,13].

In this work, a new design of configurable analogue block for FPAA based on transistor level of MOSFET operating in strong inversion will be presented. This work will utilize this method where research has not been extensively done. As this work will start the design of CAB from transistor level, no active element such as OTA or CFOA will be used in the heart of the configurable block. This will free the design from being dependent on the performance of used devices.

1.3 Methods of Configurable Analog Block Design

Over the years, various design methods for Configurable Analog Blocks (CABs) and FPAAs have been developed and reported in the literature. Some of these methods employ the discrete time domain such as switched capacitors and switched current. Other

methods employ the continuous time domain such as OTA based, CCII based, CFOA based and transistor level based design. Brief description of each method is presented:

1.3.1 Switched Capacitors Based Method

This method usually employs an Op-amp in the heart of its CABs surrounded by switched capacitors in order to implement the required function. This is considered a discrete time method due to sampled data nature employed.

This approach is well suited to digital systems designs. However, operational amplifier-based CABs suffer from the limited upper frequency range. This is attributed to the limited gain-bandwidth product of the operational amplifiers [5]. Also, the input signal frequency is limited to at least one half of the sampling frequency. In addition, anti-aliasing and reconstruction filters must be used. Moreover, the power consumption of continuous time (CT) designs can be less than a third of discrete-time (DT) realizations [3, 15]. Reported designs employing this method can be referred in [6, 16, 17].

1.3.2 Switched Current Based Method

This method is also a discrete time one. One of the switched current designs is reported in [18]. It utilizes the discrete-time current mode approach based on a current copier circuit, by recording the input current on the gate capacitance of a transistor during phase 1 and outputting a copy of that current during phase 2. The same advantages and disadvantages mentioned in the switched capacitors method can apply here. In addition, this method has the advantage of lower supply used since it is a current mode design.

1.3.3 Trans-conductance-Capacitor (G_m-c) Based Method

In this design method, the inter-connections between configurable analog blocks are realized using tunable trans-conductors. For example, in [19] the CABs consist of Op-amps and programmable capacitors, while the inter-connections are achieved using MOSFET trans-conductors.

This method exhibits improvement in the frequency & noise since it is using trans-conductor rather than switches. Furthermore, the interconnection networks can also operate as programmable functional elements. However, the required area will be more than the designs using switches.

1.3.4 Current Conveyor ($CCII$) Based Method

This method of CAB design is achieved using second generation current conveyor (CCII) as the active element in the CAB in addition to a bank of programmable resistors and capacitors. The inter-connection network is usually implemented using MOSFET switches.

The drawback of this method is that the performance of the FPAA (power & speed) will be limited by the capability of the CCII used. However, it provides better frequency performance when compared to the designs using Op-amps in their CABs. Reported designs employing this method can be seen in [9, 10, and 20].

1.3.5 Operational Trans-conductance Amplifier (OTA) Based Method

This method of CAB design is achieved using Operational Trans-conductance Amplifier (OTA) as the active element in the CAB in addition to programmable resistors and

capacitors. The interconnection network is usually implemented using MOSFET switches, however, in [21] floating gate (FG) transistors are used as switches.

The drawback of this method is that the performance of the FPAA (power & speed) will be limited by the capability of the OTA used. However, it provides better frequency performance when compared to the designs using Op-amps in their CABs. Reported designs employing this method can be seen in [4, 8, 21 and 22].

1.3.6 Current Feedback Op-Amp ($CFOA$) Based Method

CFOA based CAB design is very rare in the literature. The one presented in [7, 23] is using CFOA, a bank of programmable resistors and capacitors connected via switches. The same advantages and disadvantages of the CCII can apply here.

1.3.7 Trans-linear Elements (TLE) Based Method

CAB's built using trans-linear Elements (TLEs), as the core computational unit, has been gaining researchers attention recently. This type of CAB is either BJT or MOS in sub threshold. Ideal trans-linear elements have infinite input impedance and an exponential voltage to current relationship. In addition, any trans-linear element can be made to have multiple inputs by simply applying resistive or capacitive division at the voltage input.

This method usually uses floating-gate transistors to implement switch networks and TLEs to create reconfigurable trans-linear networks. Floating gate transistors are the normal MOS transistor with an additional floating-gate which can be programmed using Hot-electron injection and Fowler-Nordheim tunneling .These techniques introduce/remove charge at the floating gate which can be used to bias the characteristics of the floating-gate transistor. Such post-fabrication programmability of charge at the

floating-gate can be used to program the analog device characteristics such as the threshold voltage of the transistor [24].

FG transistors are very useful for switching since they do not require outer memory. In addition, the ability to program the charge on the gate of each MITE allows for the cancellation of threshold mismatch between the devices. Also, this method would allow for large scale integration of analog designs as in [12]. The major drawback of this method is that it is not using standard CMOS process [2]. Reported designs using this method can be found in [1, 13, 14, 21, 24 and 25].

1.3.8 Transistor Level or Transistor Circuit Primitive Based Method

This method does not depend on any active device in its CAB; rather it constructs the CAB from the transistor level or simple collection of transistors to form the primitive. The required functions to be achieved by the CAB are targeted in its design. The routing connection within the CAB to achieve configurability and tune-ability can be done by implementing MOSFET switches as in [26 and 27] or by digitally altering the biasing current as in [5 and 28] .

In the literature, this method was utilized in [11] implementing the design using MOSFETs in sub-threshold region. The use of pass transistors in the signal path and the sub-threshold operation has led to limited bandwidth. In [5], the design is based on BJT transistors and it is not using switches in the signal path, altering the biasing current is rather used in the CAB routing. As a result, high frequency operation was achieved. In [26] the design is implemented using MOSFETs in saturation to construct configurable

analog cell (CAC). Switches were used for configuration. The frequency reported in the last example was moderately high.

The use of this method, allows the design performance not to depend on the used active device. Additionally, the use of digitally modifying the biasing current in the CAB routing results in improvement in the bandwidth.

1.4 CAB Design Considerations

1.4.1 Continuous or Discrete Time

An important decision in the design of CAB is whether it is to be designed in the discrete or continuous time. In the literature, there are two famous approaches to design CAB's in the discrete time: the switched capacitor method or the switched current method.

Discrete-time approach is well suited to digital systems designs. However, such sampled data techniques require that input signals to be band limited to at least one half of the sampling frequency, and hence anti-aliasing and reconstruction filters must be used. This requirement often limits the bandwidth of discrete-time CAB circuit implementations.

Continuous-time circuit techniques do not impose limitation on the BW of input signals, but may require more complicated implementations to have the circuit components programmable. In addition, the power consumption of continuous time (CT) designs can be less than a third of discrete-time (DT) realizations [3 and 15]

1.4.2 Voltage or Current Mode Operation

Another important design choice is whether to use voltage or current as the signal parameter in the CAB/FPAA implementation. Voltage signals have a high fan out. In addition, voltage-mode circuit techniques are well-developed. However, Most of the existing voltage-mode CABs cannot satisfy the requirements of low power and high frequency operation. In general, voltage-mode circuits will always suffer from the need of higher power supply voltages to maintain reasonable dynamic ranges [3 and 5].

On the other hand, current-mode circuits can work at higher frequencies than voltage-mode circuits and require less power supply voltage. In addition, current mode circuits are simpler in implementation of many circuits and have higher accuracy. Moreover, recent trends towards lower power supply voltages have reduced the dynamic range available in voltage-mode circuits, making current-mode signaling more attractive. As a result, current-mode CABs would be more appropriate to adopt, especially for high frequency operation [3 and 5].

1.4.3 Other Considerations

Design of CAB is also influenced by a number of factors, including the functionality and performance features of circuits, the area-efficiency and the supporting semiconductor process technology. Another key issue in CAB design is the level of granularity. Fine grain CAB's architectures (reconfigured at low level, e.g. transistor level) will require more routing resources and will have more switches in the signal path than a coarse grain CAB architecture (reconfigured at a macro-block level, e.g. integrators, S/H). However, the coarse architecture will be less versatile i.e. it will be able to implement a narrower range of circuits than the fine architecture [3].

1.4.4 Interconnection Architecture and its Implementation

There are two types of interconnection (routing network): Internal routing, which is used inside the CAB to connect its components together and the external routing, which connects the CABs together to form a complete FPAA. The choice of an interconnection architecture and its implementation will influence the rout-ability of prototyped circuits and their performance. Pass transistors and CMOS transmission gates have been used as switches to reconfigure the topology of the circuit being implemented [3].

There are two architecture schemes of interconnections that opposed to each other. One is based on providing programmable connections between every pair of cells in the circuit. This approach favors flexibility, but also leads to excessively long signal interconnections, which introduce phase errors and cross talk problems for the circuit operation at high frequencies. The second scheme is based on restricting the interconnection pattern in favor of better high frequency performance [4].

In local connection topology, each cell can receive output signals only from the nearest neighbors, and can send its own output signal to the same neighbors. Given adequate functionality of each cell, this restricted topology allows implementation of various important classes of circuits.

Although a wide variety of applications can be realized in this locally-only interconnected architecture, some circuits require global connections. It can further enable implementation of other circuits, such as matrix operations circuits.

Some reported designs have made circuit structure reconfigurable without the use of extra switches in the signal path, by the use of discrete-time sampled-data techniques.

Alternatively, signals can be coupled from one CAB to another or within the CAB without reconfiguration switches in the signal path by changing the bias of an interface circuit such as a current source [3].

CHAPTER 2

LITERATURE REVIEW

Since the early 90s of the past century, researchers started to develop many designs of FPAA's. These designs vary in their complexity, range of applications and the design method used. Some of these designs were converted into commercial products but most designs were not. This section will report some important examples of the commercially available FPAA's and the academically reported FPAAs.

2.1 Commercial FPAA Designs

2.1.1 EPAC Design by IMP

In 1996, IMP released the first commercially available FPAA (EPAC), electronically programmable analog circuit, which was a large step in analog system design. This device design was aimed towards general signal conditioning, data communication, data/signal monitoring. Each CAB of EPAC design uses an Op-Amp to perform operations like amplification and comparison while switching capacitor method is used to program the individual CAB's; therefore it is classified as discrete time design. The data for the CABs is stored in (EEPROM) and loaded into static random access memory (SRAM) when the device is started up [2 and 6].

The performance of EPAC IMP50E10 when used as multisensory analog front end to an A/D converter in a battery charger application was illustrated in [6]. In the mentioned example, some key performance parameters were reported such as: $\text{supply voltage} = 5\text{V}, \text{max signal BW} = 125\ \text{kHz}, \text{max output current} = 40\ \text{mA}, \text{max dynamic range} = 100\text{db}$ and $\text{THD} = -68\text{dB}$.

Due to the use of Opamp and the SC technique as shown in figure (2.1), EPAC is very limited in BW.

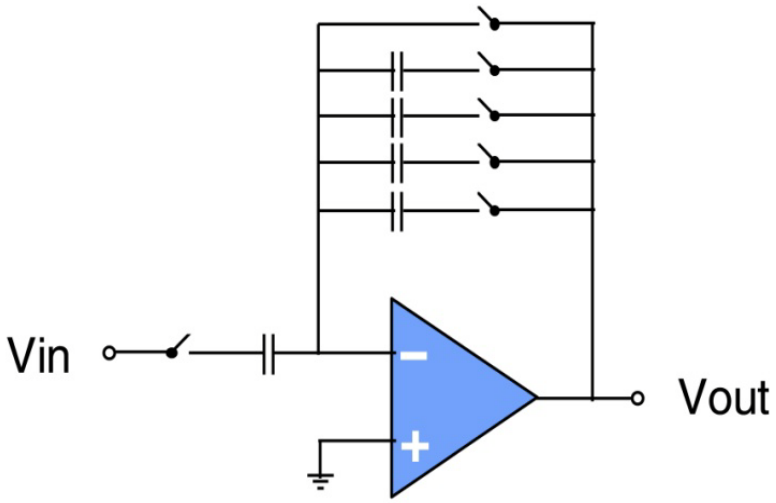


Figure 2.1 EPAC switched capacitor implementation concept [6]

2.1.2 TRAC Design by Zetex

The first commercial continuous- time FPAA was announced by Zetex in 1996[3].The totally reconfigurable analog circuit (TRAC) design was implemented in bipolar technology (log domain). The TRAC consists of 20 CABs in two rows of 10, each of which can be configured to implement one of six functions, namely Add, Negate, Pass, Log, Antilog and Rectify. Each CAB is based on Op-amp connected to internal/or external components to achieve the configured function. On-chip interconnections are local only, with the output of each cell connected to the input of the next. The inputs and outputs of all cells are brought off-chip to enable global routing using external connections and/or components.

When the TRAC FPAA was configured to work in filter application, it was reported to consume 18 mW of power and work up to 12MHz.

One of the serious drawbacks to the TRAC design is that most of the interconnections between CABs need to be wired externally, rather than programming them on the chip [2, 3 and 29]

2.1.3 IspPAC Series Designed by Lattice Semiconductor

Lattice Semiconductor produced three types of the IspPAC series IspPAC10, 20 and 80 which were intended for signal processing and conditioning applications. The Lattice structure includes four instrumentation amplifiers, DACs and Op-amp's allowing the IspPAC to implement amplifiers, filters, integrators or comparators, see figure (2.2). This series of FPAA employs the continuous time processing technique.

The IspPC10 allows for implementation of a filter with corner frequency ranging from10 KHz to 250 KHz. However, In 2007 Lattice discontinued the IspPAC series of FPAAs, and consequently they are currently unavailable [2, 30].

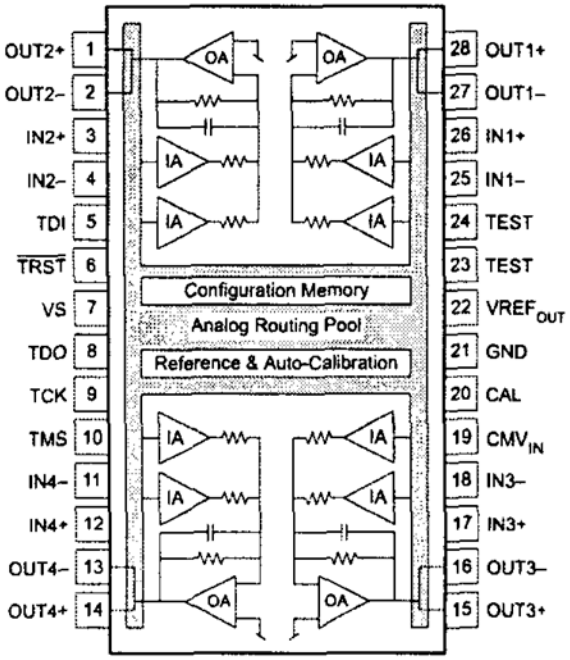


Figure 2.2 IspPAC10 block diagram [3]

2.1.4 MPAA Design by Motorola

The core cell of Motorola MPAA020 FPAA design is based on switched capacitors technique. It contains 20 switched capacitor (SC) cells with the Programming data held in SRAM in each cell. Each cell contains Op-amp, comparator and capacitors. Each core cell is capable of a number of primitive functions such as gain, rectification and first order filtering. The majority of the interconnections between cells are local, to allow a core cell to directly communicate with the cells adjacent, but global interconnections are also available.

The MPAA020 is capable of supporting a diverse range of analogue signal processing functions, such as data conversion, linear signal processing, filtering and non-linear functions.

The discrete time analog design, resulting from the use of switched capacitor circuits, limits the bandwidth of the circuits implemented on the FPAA [2 and 16].

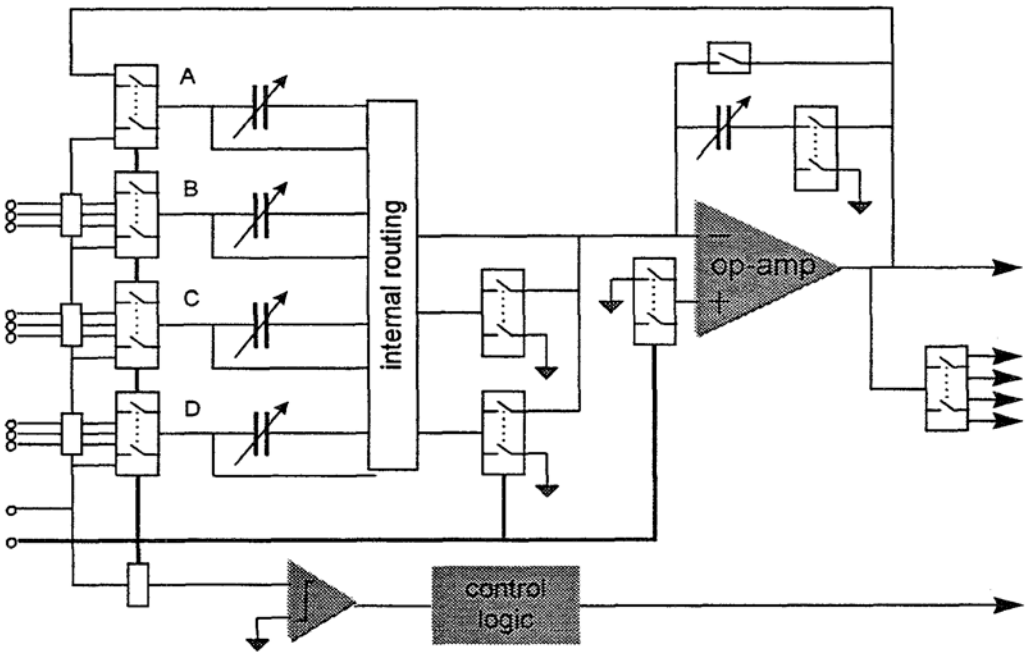


Figure 2.3 MPAA switched capacitor core cell [16]

2.1.5 Anadigm AN10E40 Design

The Anadigm AN10E40 is another Switched Capacitor based design. AN10E40 is very similar in design to the Motorola MPAA020, but it does not have a comparator. As with the Motorola design, there is no onboard non-volatile memory on the AN10E40, and as a result configurations must be stored off-chip, and loaded into the onboard SRAM at start-up [2 and 15].

2.1.6 RASP 2.8 Design

Reconfigurable Analog Signal Processor (RASP) design is one of the most advanced designs in literature. This design by Basu et al. provides a large array of 32 CABs and uses floating-gate transistors to implement the programmable interconnects and circuit elements .The CABs are of two major types, the first one has three OTAs, three floating capacitors, two multi-input floating gates, a voltage buffer, a transmission-gate and NMOS/PMOS transistor arrays .The second type of CAB has a folded Gilbert multiplier in addition to a wide linear range OTA [2 and 21]. This design of FPAA can achieve BW over 59MHz [21].

The commercially available FPAA's are summarized in table (1).

Table 1 Commercially available FPAA designs [2]

Company/Author	Product	CAB Design	Technology	Application	BW
Lattice [30]	IspPAC	Op-Amp	CMOS	Signal processing and conditioning	250KHZ (IspPAC10)
Zetex [29]	TRAC	BJT Op-Amp (Log domain)	Bipolar	General signal processing	12 MHz
Motorola [16]	MPAA020	SC/Op-Amp and comparator	CMOS	General signal processing	200 kHz
IMP [6]	EPAC	Switched Capacitor/Op-Amp	CMOS	Signal conditioning and monitoring	125kHz
Anadigm [2]	AN10E40	Switched Capacitor/Op-Amp	CMOS	Signal processing and conditioning	----------
A. Basu & C. M. Twigg [21, 31]	RASP 2.8	Floating Gate OTA	Floating-Gate CMOS	Signal Processing	50 MHz

2.2 Academically Reported FPAA Designs

2.2.1 MOSFET Sub-threshold Design by Lee and Gulak

Lee and Gulak developed a low-power FPAA based on MOS sub-threshold circuit techniques designed at transistor primitive level. Their work employed both voltage and current-mode circuits and was designed to implement structurally and parametrically reconfigurable circuits. Since their design was mainly aimed towards neural networks application, the designed CAB is capable of performing addition, threshold operation, coefficient multiplication and signal multiplication. This FPAA is designed to operate below 100 KHz frequencies [32].

The CABs of this design were built from other sub-blocks. The internal routing of the CAB is determined by a local 3-b shift register. Pass transistor switch networks were used as the active switch elements to connect the sub-blocks as shown in [11].

The experimental prototype is fabricated in 1.2μm CMOS technology. The linearity was measured to have maximum of 2% error. Since sub threshold circuit technique is used, the designed FPAA offers the advantage of low power dissipation [3 and 11]. On the other hand, the use of pass transistors in the signal path, limited the design BW due to parasitic effects [32].

2.2.2 Trans-conductor Based Design by Lee and Gulak

A MOS trans-conductor based FPAA has been described in the literature. It consists of four CABs each of which has operational amplifiers and programmable capacitors. The connections between configurable analogue blocks are realized using MOSFET trans-conductors.

This FPAA was designed to implement applications in the area of analog signal processing in 100kHz range [32]. A fully functional prototype, fabricated in a 1.2μm CMOS process, was reported. The reported FPAA dissipates less than 80mW of power.The THD is less than −57dB at 1kHz for a 1.6V peak-to-peak output swing [3, 19, 33 and 34].

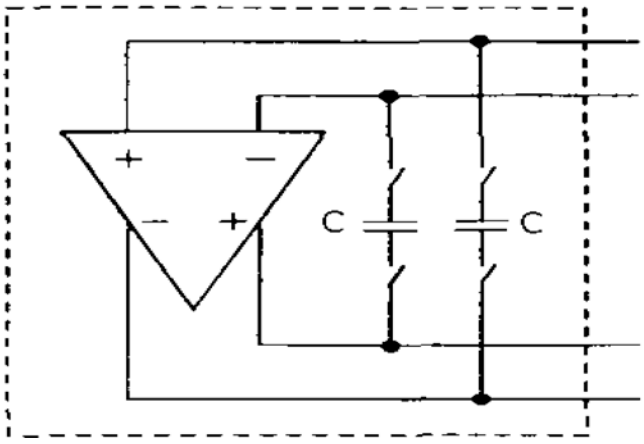


Figure 2.4 CAB schematic diagram [19]

2.2.3 Switched Capacitor Based Design by Kutuk and Kang

This design of an FPAA is based on voltage-mode switched capacitor techniques. It is designed to operate at frequencies up to 125 kHz .Each CAB in the design contains a lossless integrator and a lossy integrator, implemented using switched capacitor techniques and Op-amp's. Both integrators are connected in looping structure which gives the CAB a second order nature. The interconnection network between CABs in the

FPAA was composed of switched and un-switched capacitors. The internal structure of CABs and the interconnection network between them are configured by user-programmable digital control signals.

In [17] Simulation results were given for circuit embeddings of a third-order low-pass elliptic filter, a fourth-order band-pass filter, a balanced modulator and a sinusoidal generator [3 and 17]

2.2.4 Switched Current Design by Researchers of Nottingham University

A design methodology for building switched current circuits using a four phase clock is proposed in [18]. The switched current technique is a discrete-time current mode approach based on a current copier circuit, by recording the input current on the gate capacitance of a transistor during phase 1 and outputting a copy of that current during phase 2.

In this design the set of functions to be performed by the CAB are:

1. Current copier with programmable gain and phase.
2. Programmable phase current comparator.
3. Programmable output switch.
4. Programmable current reference.

The CAB was fabricated using 0.7μm CMOS and test results for applications of current control oscillator and LPF are presented [3 and 18].

2.2.5 Current Conveyor Based Design by Gaudet and Gulak

Gaudet and Gulak presented a CAB for FPAA that is based on current conveyors. This FPAA is targeted toward applications in the video frequency range (10 MHz). The designed CAB consists of a second generation current conveyor (CCII) and a bank of programmable resistors and capacitors. The function set adopted for the CAB includes integration, differentiation, and amplification [20 and 32].

An IC test results of a 0.8μm CMOS chip containing four configurable analog blocks based on the CCII are presented in [20]. Frequency response shows that the $-3dB$ points for various gains were measured at11 to $13MHz$. The total harmonic distortion was measured at 2.89% for 10 kHz $0.5Vp-p$ input sine wave. Power dissipation was at the level of is $162mW$ for $5V$ supply.

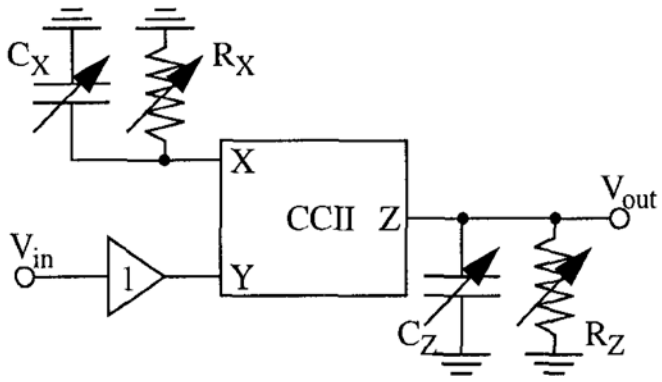


Figure 2.5 CCII based CAB [20]

2.2.6 BJT Operational trans-conductance amplifier Design by Researchers of Portland University

The research group of Portland State University presented a bipolar current-mode Continuous-time OTA-based Design .The architecture of this FPAA has a matrix-like topology that consists of current-mode processing CABs interconnected to each other using a two levels routing network; local and global. Each CAB is composed of control block, 2 summers, multiplier, integrator/amplifier and 2 limiting clipping clocks. One of the most important configurable blocks forming this cell is the current-mode integrator/amplifier configurable circuit .This CAB is based on OTA-C technique in which the configuration is done using biasing currents rather than switches. However, the capacitors used in this design are floating capacitors making the circuit subject to parasitic effects .This FPAA is mainly targeted toward continuous, fuzzy, and multi-valued logic applications [4 and 32].

The frequency range of this FPAA is up to 10 MHz .The design works in one of two modes: passive-control mode and active-control mode. In the passive control mode only the analog blocks of the cell perform signal processing functions. The control circuit determines the parameters and configuration of the analog blocks, but not involved in the signal processing. In the active-control mode, the control circuitry additionally takes part in some signal processing functions [4 and 32].

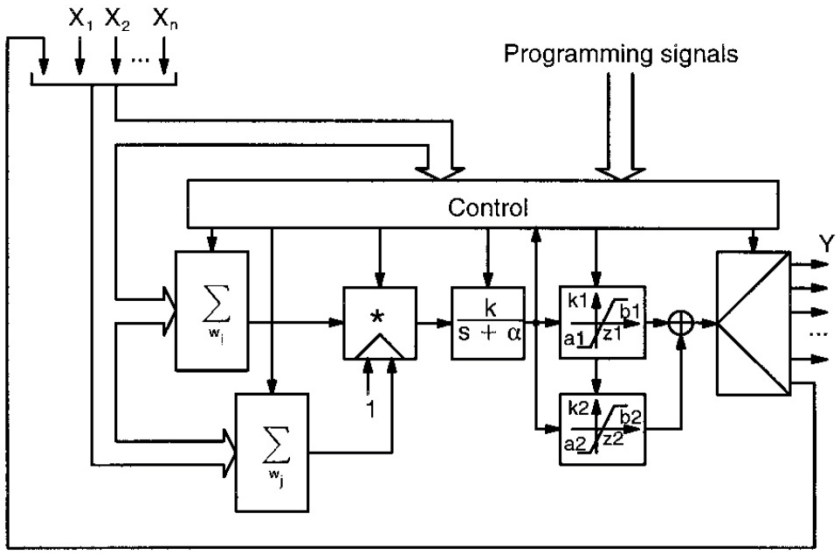


Figure 2.6 Functional block diagram of programmable cell [4]

2.2.7 Configurable Analog Cell Based Design by Researchers of Texas University

Another research group proposed a current-mode FPAA that consists of a modular array of CABs each of which includes three sub-cells: a Configurable Analog Cell (CAC), a Programming Register (PR), and Programming Logic (PL). The CAC is designed so that it can be configured to perform one of three functions: integration, amplification, or attenuation. The programmability for both the functionality and the parameters can be achieved by activating and deactivating certain branches forming the CAC itself via switches.

The proposed FPAA has been designed in a 2μm orbit digital CMOS process. It has been demonstrated that this design can operate over almost 3 decades of frequency range (30 kHz to 10MHz) [26, 27 and 32].

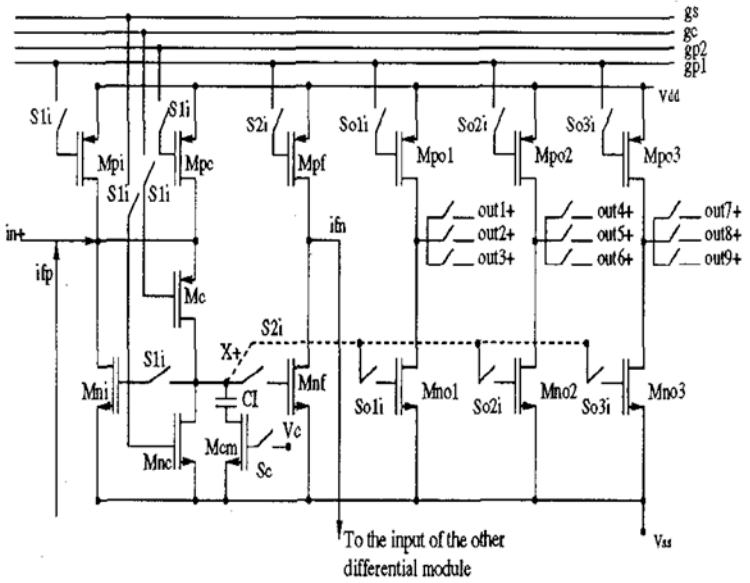


Figure 2.7 CAC circuit schematic [27]

2.2.8 OTA Based Design by Researchers from the Universities of Gdansk and Hertfordshire

Another research group presented a general CAB that consists of a programmable OTA, programmable capacitors and MOSFET switches. Based on this CAB a universal 5x8 CAB array has been simulated and fabricated.

Simulations and experimental results show that filters with frequencies from several kHz to a few MHz can be realized based on this CAB. The fabricated array has been configured to realize OTA-C 60kHz and 500kHz band-pass filters [8, 22 and 32].

2.2.9 Current Conveyor Based Design by France Research Group

A research group in Cimirly Lyon, France has developed a current conveyor-based FPAA [9, 32 and 35]. For details of this design see table (2).

2.2.10 Transistor Level BJT Based Design by Abulmaati and Fares

In this design a current-mode configurable analog blocks for FPAA is reported. The configurable blocks are capable of performing integration, differentiation, amplification, pass and exponential functions in addition to add and subtract functions that can be easily realized in current-mode circuits. This set of functions is the same as the one adopted by the commercially available TRAC FPAA However, the proposed CABs use transistor based current-mode continuous-time approach utilizing the bipolar junction-transistor (BJT) trans-linear principle [5 and 32].

In order to get the maximum possible bandwidths of these cells and for the design not to depend on the used device's bandwidth but on the transistor's characteristic, these cells are designed on the transistor level utilizing the trans-linear Principle (TLP). In addition, the programmability and configurability of the blocks are achieved by digitally modifying the block's biasing conditions [5 and 32].

Based on the designed CAB, a universal second order filter using at most four CABs has been simulated. The results of the five standard filter functions low pass, high pass, band pass, notch and all pass has been reported in [28]. The four CABs were connected in a string-like topology. The reported results show that HP filter was simulated at 50 MHZ with non-linearity error of 2% in the passband, the LP filter was simulated at 3MHZ with non-linearity error of 3% in the passband and the BP filter was simulated for a center

frequency of 8.7MHz with non-linearity error of 2%. The maximum upper frequency achieved here was in the case of the LPF realization and it was around 100 MHz [28].

In all the simulation results, the major limitation on the frequency is the transistor cut off frequency (f_T), so it is expected that if a transistor with wider (f_T) is used the BW will increase. The high BW achieved was also due to that the internal routing of the CAB is done via changing the bias condition of the circuit. This avoids the use of capacitor- and/or resistor-banks and the relatively large number of switches needed for programming the CABs Thus, reducing the required silicon area for integration and achieving higher frequencies of operation [5].

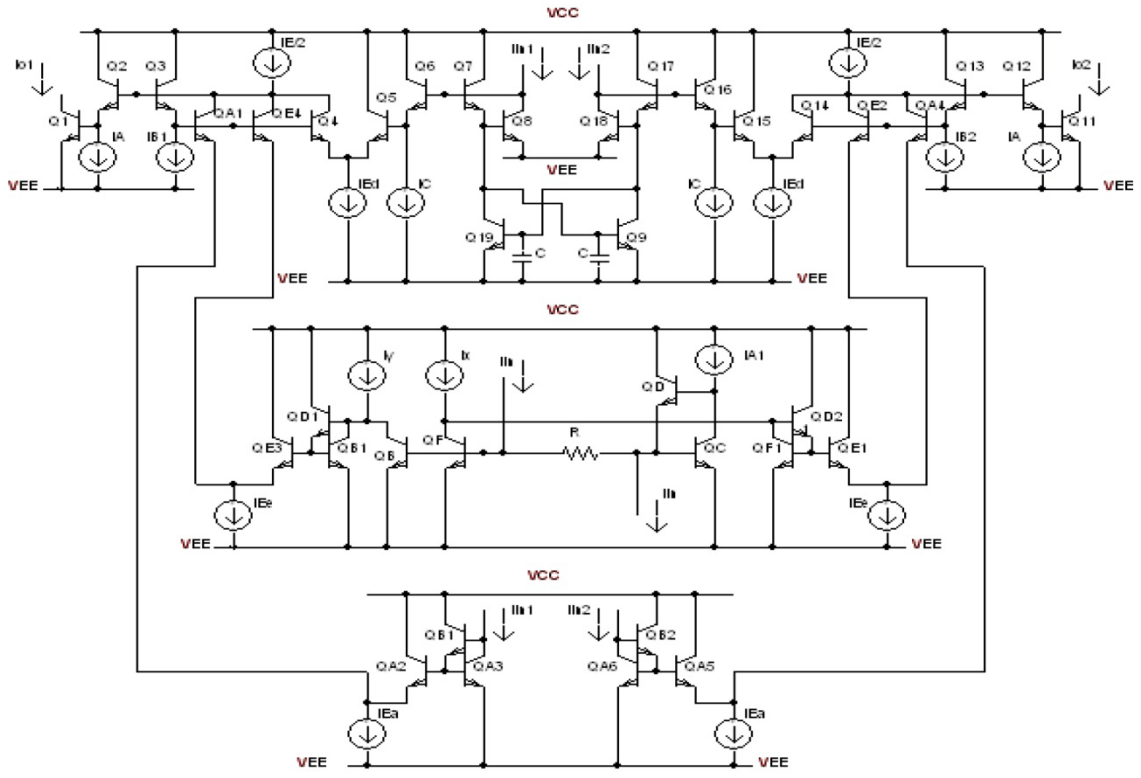


Figure 2.8 Part of the CAB circuit for differentiation, exponential and pass function [5]

2.2.11 Multi Input Trans-linear Element Based Design by Schlottmann, Abramson and Hasler

Large-scale trans-linear FPAAs can be built using floating-gate transistors as both the computational elements and the reconfigurable interconnect network. An FPAA built using multiple Inputs trans-linear Elements (MITEs), as the core computational unit, has been designed, fabricated in 0.35 μm CMOS, and tested. These devices have been programmed to implement various circuits including multipliers, squaring circuits, RMS-to-DC converters, and filters.

This type of FPAA is either BJT or MOS in sub threshold. Ideal trans-linear elements have infinite input impedance and an exponential voltage to current relationship. In addition, any trans-linear element can be made to have multiple inputs by simply applying resistive or capacitive division at the voltage input.

In order to allow for the practical Implementation of this FPAA in a simple digital process, sub-threshold pFETs has been chosen to be used. This pFET has a current that is exponentially related to its gate voltage. Each CAB contains two of the MITE elements, a first-order log-domain filter, six bias current generators, six nFET mirrors, and a cascade – bias generator.

The interconnection architecture of this FPAA was designed using the floating-gate switch matrix framework of the RASP 2.8. The RASP infrastructure incorporates a cross-bar switch matrix for connecting the elements to one another. The connection between the horizontal and vertical line is controlled by a single floating-gate switch, which allows it to store its own value without a separate memory.

In this FPAA 18 CABs in 6x3 array has been used with 17 being MITE CABs and one being the I/O CAB. The layout of this FPAA was fabricated in $0.35\,\mu m$ CMOS with $V_{dd} = 2.4V$.

The first function tested on this design was a first-order low-pass filter. The highest achievable corner frequency is200 KHz. Next, a first-order high-pass filter was compiled onto the FPAA. The filter was built by subtracting a low-pass filtered version of the input from the original signal. Also, an RMS-to-DC converter was also compiled. The BW of the chip was measured to be 200 kHZ and the current range is from $1nA$ to $1uA$ since it operates at sub-threshold [1].

2.2.12 Trans-linear Element (TLE) Based Design by Abramson

This design introduced a CAB that uses trans-linear elements as computational unit. The system uses floating-gate transistors to implement switch networks and MITEs to create reconfigurable trans-linear networks. The system architecture includes 3 MITEs CABs, 1specialized CAB for implementing four quadrant and dynamic functions, and a global switch matrix.

Multiple-input trans-linear elements (MITEs) were chosen as the core of the system blocks. The design is broken up into three core structures: global switch matrix, MITE Configurable Analog Blocks (CAB), and a specialized CAB. An MITE CAB consists of 8 MITEs. Both the global switch matrix and all of the local switch matrices in the CABs are full crossbar switch networks.

The chip was fabricated in a 0.5μm process and several circuits were programmed onto the system and results were taken for each. Some of the circuits built were the squaring circuit, a square root function, a 2nd order trans-linear loop, square and a square root function and finally, a 1st-order log-domain filter. The cut off frequency for results reported is less than 1 kHz [13].

2.2.13 Reconfigurable Trans-linear Cell Based Design by Alvarado

This design aims to build an FPAA based on reconfigurable Trans-linear Cell (RTC) to be used in the application of signal processing. An Array of 5x5 CMOS RTC was designed .Each trans-linear cell contains a trans-linear element (TE), a programmable current mirror (PCM) block, programmable current sources (PCS) blocks, a programmable capacitor (PCAP) block, three switch matrices (SM), a configuration memory (REG), configuration switches and an additional MOS transistor.

Using the RTC, some useful circuits have been generated such as a four-quadrant multiplier, and a fourth-Order low-pass filter tuned at different cut-off frequencies. The band width of the system was reported to be about 7 MHZ [14 and 25].

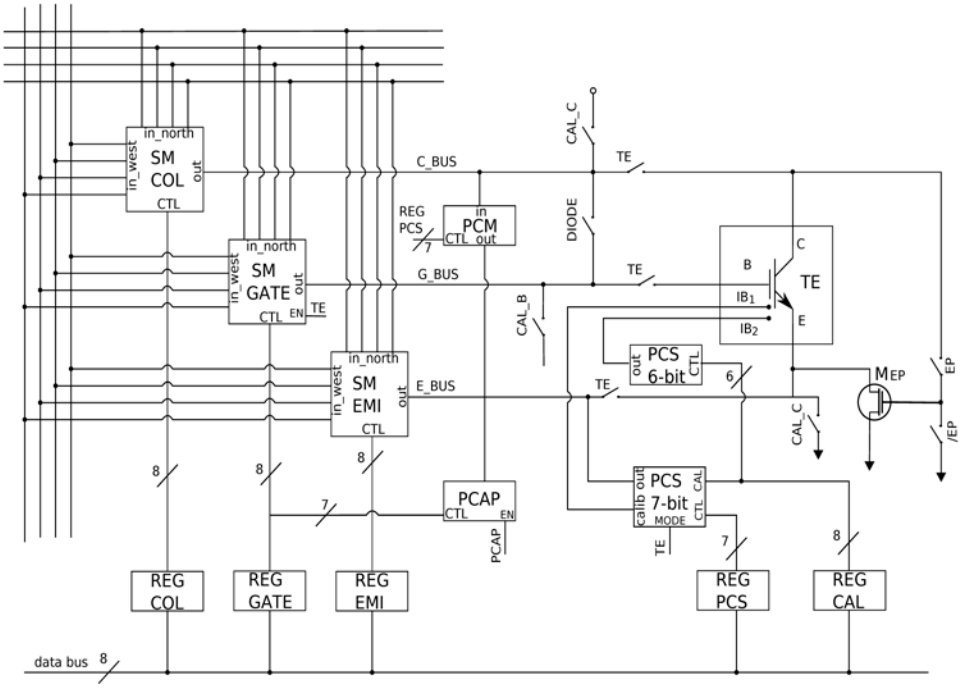


Figure 2.9 RTC architecture [14]

The academically developed FPAA's, mentioned above and other reported in the literature are summarized below in table (2).

Table 2 Academically reported designs [32]

Reference	Approach	Programmability & Configurability	BW	Notes
[11]	CMOS Sub-threshold-Transistor primitive based.(1.2µm CMOS)	Pass transistor switch	Below 100kHz	Low power, limited BW, Neural net. app.
[19, 33, 34]	Op-Amp &programmable C's. (1.2µm CMOS)	CMOS Trans-conductors as switches.	Around 100kHz	Limited linearity and bandwidth
[20]	CCII & programmable R's and C's.(0.8µm CMOS)	Banks of programmable R 's & C's	Around 10MHz	Large area, video freq.app.
[26,27]	Current mode, transistor primitive based, Current-mode, 2µm CMOS.	Branch activation via Transistor switches	10 MHz	Operates in saturation.
[8, 22]	programmable OTA & capacitors (2µm CMOS strong inversion)	Programmable capacitors & MOS switches	Few KHz to few MHz	continuous signal processing
[9]	CCII based approach	Tunable resistors & capacitors.	Few kHz to few MHz	continuous signal processing
[17]	Voltage mode, S/C approach and Op-amp's.	Switched & un-switched C's.	125 kHz	Limited BW, used in signal processing
[4]	Transistor based current mode & OTA-C	Programmable biasing current	10MHz	Cont, fuzzy, and multi-valued logic app. Floating C's causing parasitic.
[18]	discrete-time switched current based on current copier(0.7µm CMOS)	CMOS transmission gates	--	--
[5, 28, 32]	Current mode BJT, transistor level.	modifying block's biasing conditions	100 MHz in BPF	Used in universal filter application.
[1]	MITE approach using sub-threshold pFETs.	Floating gate transistors.	200 kHz	LPF,HPF and RMS to DC converter
[13]	MITE approach	Floating gate transistors.	1 kHz	Squaring, square root and 1st order filter circuits used.
[14, 25]	Trans-linear element (TLE)	MOS switch	7 MHz	Signal processing.
[7, 23]	CFOA, programmable R's & C's (0.35µm)	MOS pass transistor switch.	11.3 MHZ	signal processing and filtering
[15]	17cells of Gm-C digitally tuned, in hexagonal shape.	Switchable unit-trans-conductors by digital input.	200 MHz	HF filters, high power consumption (1 W at 1.5 V)
[12]	Floating gate transistors (more than 50,000 ones).	Floating gate transistor.	5 MHz for LPF	Signal processing, Each CAB has various sub-circuit,
[10]	Voltage mode Digitally Programmable CCII FPAA (90nm CMOS)	Direct wiring	11.6 MHz	FPAA seven CAB's arranged in letter "I" structure.

CHAPTER 3

PROPOSED CAB DESIGN

This chapter explains the proposed architecture of a single CAB which is based on current mode MOSFET transistors in strong inversion. Programmability of the CAB function and tunability of some parameters are done by modifying the circuit bias condition in addition to the use of switches in some portions.

The adopted mathematical functions each CAB is capable to perform are: Addition, Subtraction, Pass, Integration, Multiplication and Division.

The design of the configurable analog block consists of:

- Three functional cells.
- Biasing - programming circuits and switches.
- Supplementary circuits such as current mirrors and tuning circuits.

Each of these parts will be explained in the coming sections. The simulation results are obtained using Tanner EDA Tools v13.0 with level 49 model parameters (BSIM3) in $0.35\mu m$ standard CMOS technology.

3.1 Functional Cells Design

The functional cells design is based on transistor level. There are no readymade active blocks such as CCII, OTA, CFOA or Op-Amp is used in the design. This is to get the

maximum possible bandwidth of the CAB and for the design not to depend on the used device's bandwidth but on the transistor's characteristics. These functional cells are:

- Addition and subtraction cell (A/S cell)
- Integration cell (INT cell)
- Multiplication/division cell (M/D cell)

The (A/S) cell can perform pass, addition or subtraction while the (INT) cell can perform either pass or integration. The (M/D) cell can perform pass or multiplication/division.

3.1.1 Addition and Subtraction – (A/S) Cell

Since current mode is adopted in the design, addition and subtraction circuits can be done rather easy. However, this circuit is programmable so it can function as adder, subtractor or pass based on user's requirements. In addition, it avoids using switches in the signal path while selecting a function. Rather, based on user's digital bits, activation and deactivation of certain biasing branches in the circuit is done which selects the function required. As a result the cell will definitely involve more circuitry compared with simple addition and subtraction current mode circuits. The circuit in figure (3.1) represents the cell. It consists of biasing current sources and cascade current mirrors. Biasing currents $I_{b1} - I_{b3}$ are always active, while the rest determine the function achieved as in table (3).

Table 3 Programming addition/subtraction cell using biasing currents

Function	I_{s1}	I_{s2}	I_{s3}	I_{a1}	I_{a2}	I_{a3}
Pass($I_{out} = I_x$)	OFF	OFF	OFF	OFF	OFF	OFF
Addition($I_{out} = I_x + I_y$)	OFF	OFF	OFF	ON	ON	ON
Subtraction ($I_{out} = I_x - I_y$)	ON	ON	ON	OFF	OFF	OFF

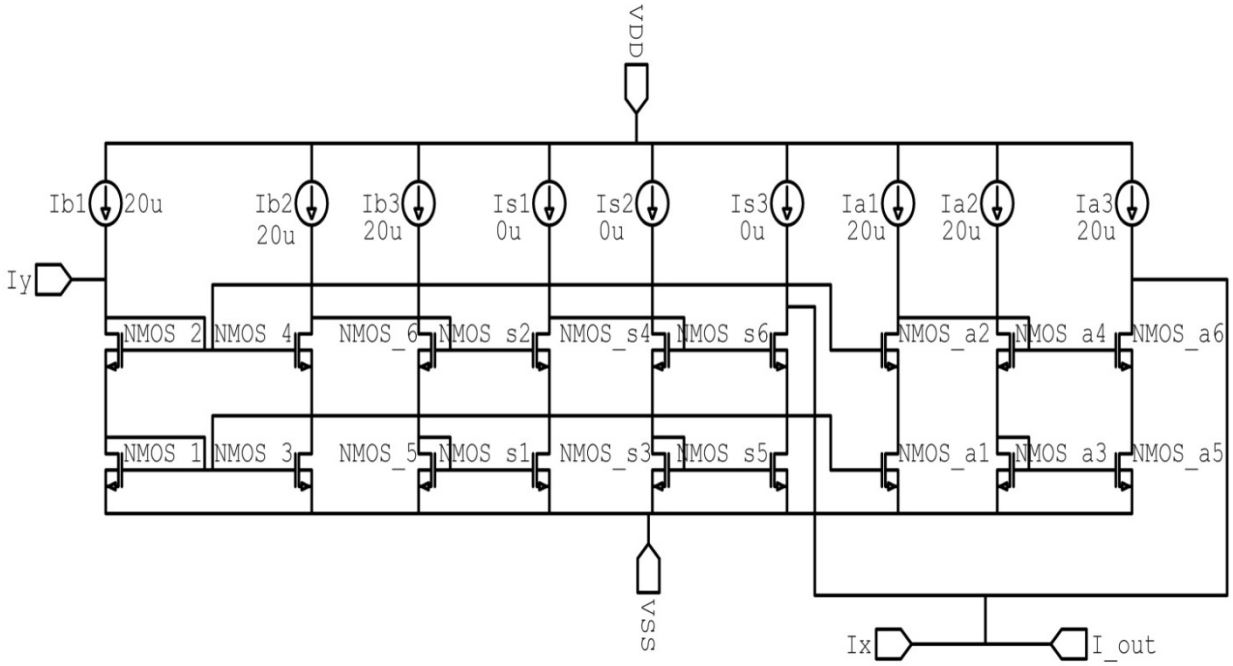


Figure 3.1 Addition-subtraction cell

Setting $I_{s1} - I_{s3}$ and $I_{a1} - I_{a3}$ off, will cause zero current flowing from the circuit into I_x node resulting to pass it through I_{out} .The Addition case is achieved by setting $I_{s1} - I_{s3}$ to zero in order to ensure that no current is flowing from the drain of $NMOS_{s6}$ to the output node. At the same time, $I_{a1} - I_{a3}$ are kept ON to deliver a copy of I_y to I_x node.

In the subtraction case, an inverted copy of I_y is delivered to I_x node while no current is flowing from the drain of $NMOS_{s6}$ to the output node. Since one of three operations can be selected, two binary bits from the user are needed to define the required function.

In order to make the circuit in figure (3.1) suitable for use in the CAB, the biasing currents have to be programmable (ON or OFF) in order to determine the state of the circuit (Addition, subtraction or pass). This feature will be integrated in the circuit in section 3.2 of this report.

Simulation results of the circuit are reported in this section. These results are obtained at the following circuit parameters: transistors aspect ratio $W/L = 5\mu/0.5\mu$, all biasing currents$= 20\mu A$ or $0\mu A$,V_{dd} & $V_{ss} = \pm 1.5V$, $R_{Load} = 1k\Omega$.

Figures (3.2-3.4) show the DC transfer characteristic of the cell when configured as adder, subtractor and pass respectively. The reported linearity errors in the three cases are 0.065% for addition, 0.075% for subtraction and almost 0% for pass. The power consumption in each case is $170\mu W, 170\mu W$ and $84\mu W$ respectively.

Figure (3.5) show the two inputs to the cell as sinusoidal wave forms. Input I_x has amplitude of $10\mu A$ and frequency $1MHz$ while I_y has amplitude of $4\mu A$ and frequency$1MHz$. The resulting output is shown in figure (3.6) for the three functions.

Figure (3.7) show the magnitude and phase frequency characteristic of the circuit for the addition and subtraction case. The $-3dB$ bandwidth achieved is $550MHz$.

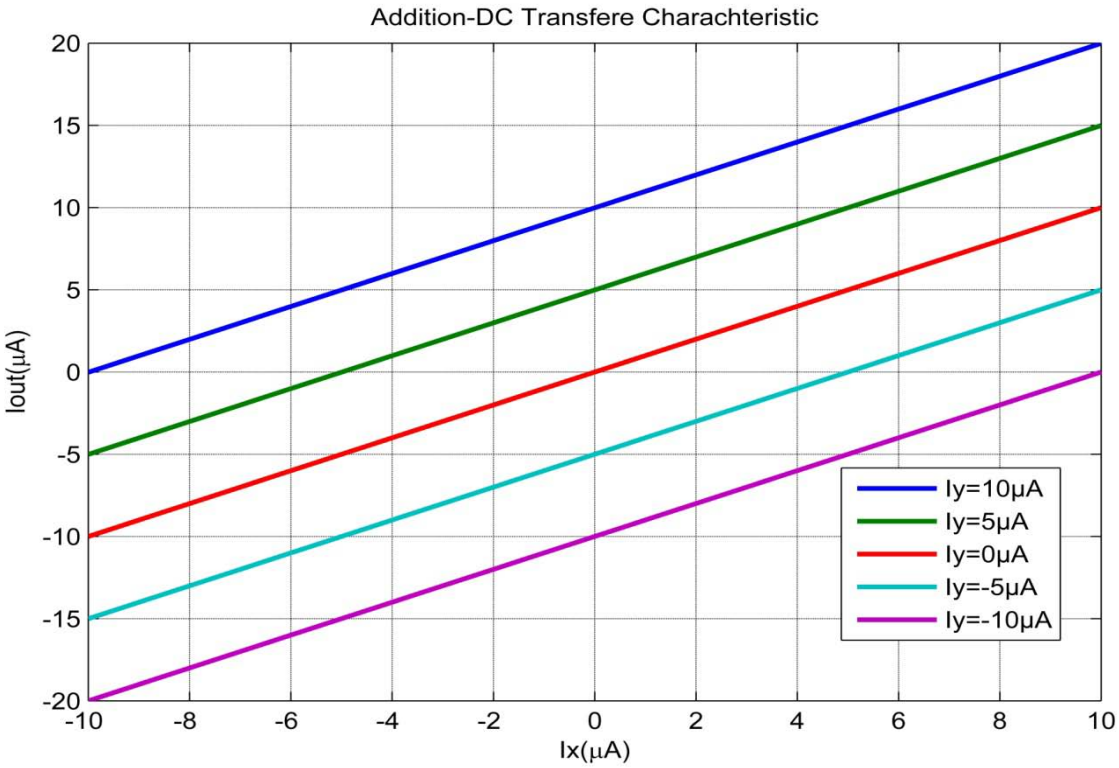


Figure 3.2 Addition DC transfer characteristic for A/S cell

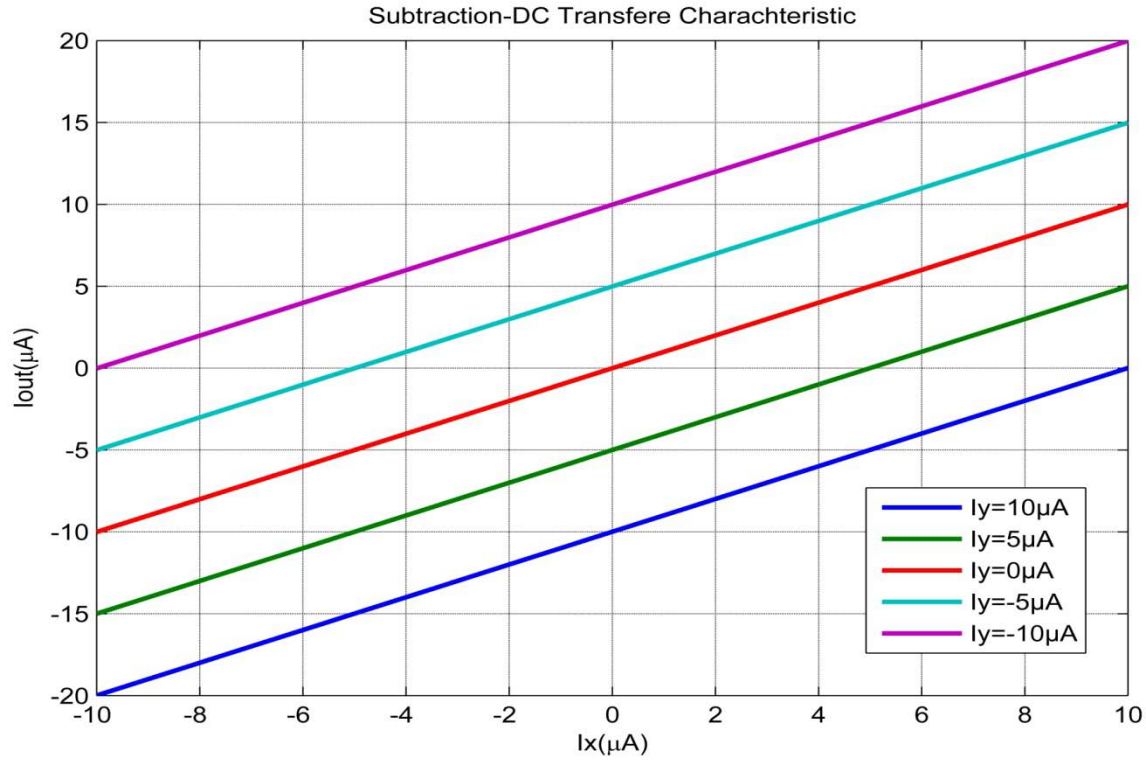


Figure 3.3 Subtraction DC transfer characteristic for A/S cell

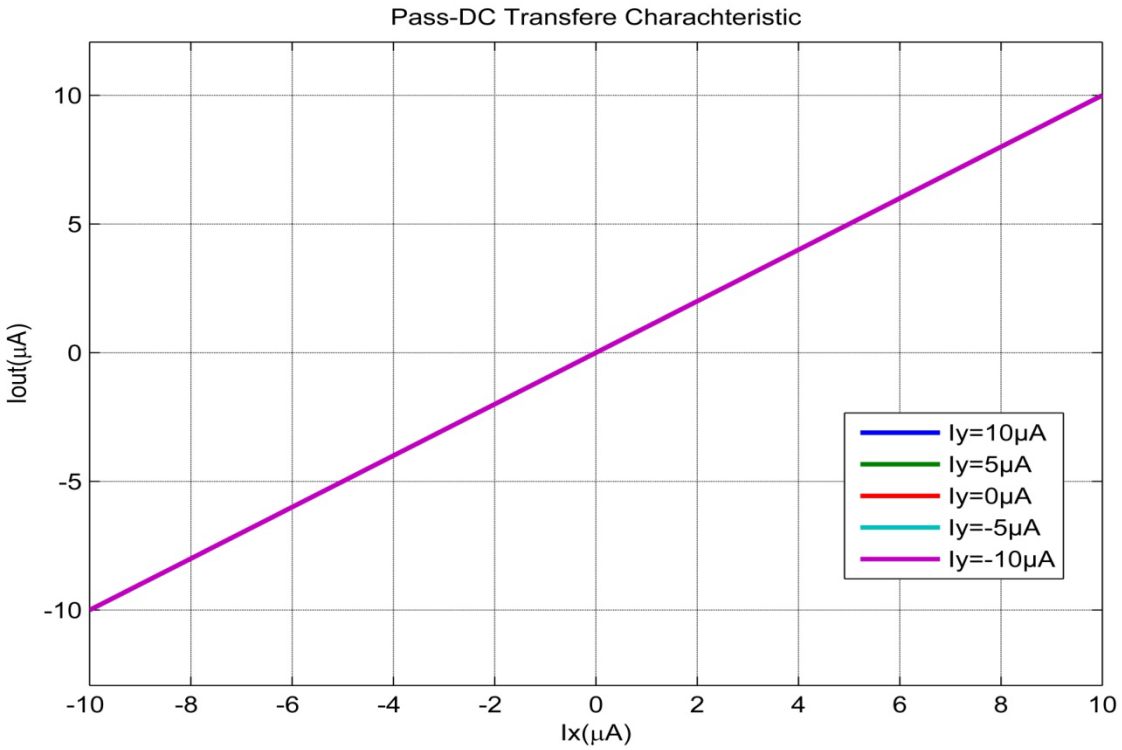


Figure 3.4 Pass DC transfer characteristic for A/S cell

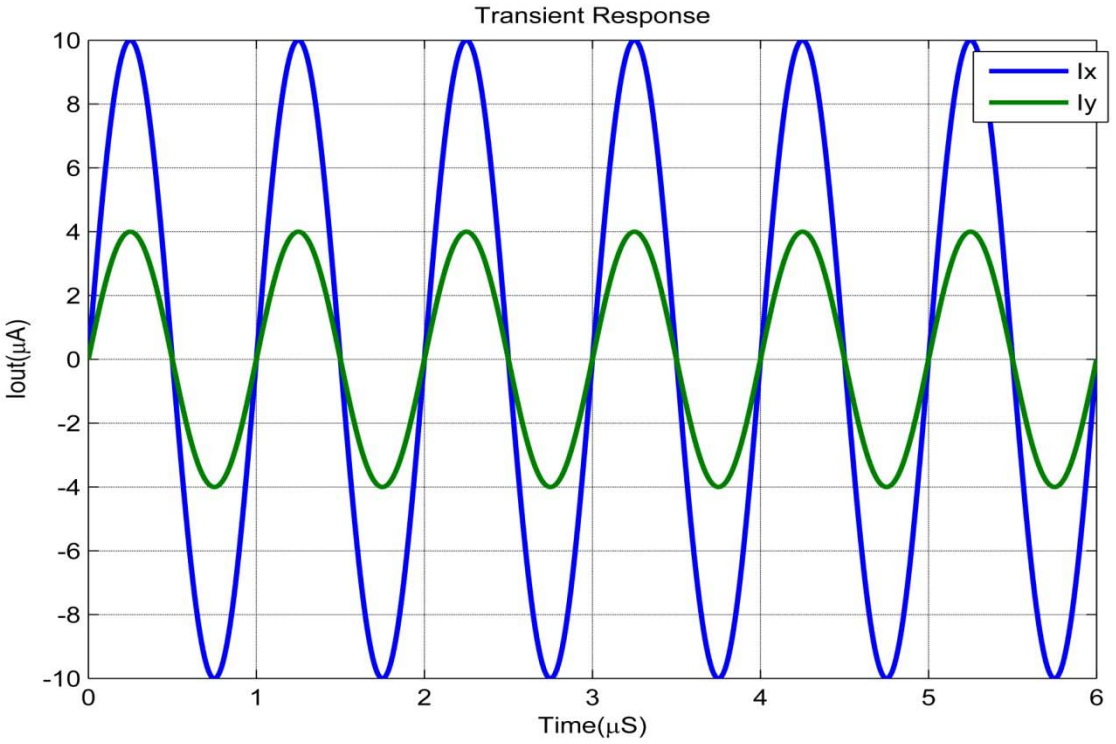


Figure 3.5 Waveforms of input currents Ix and Iy to the A/S cell

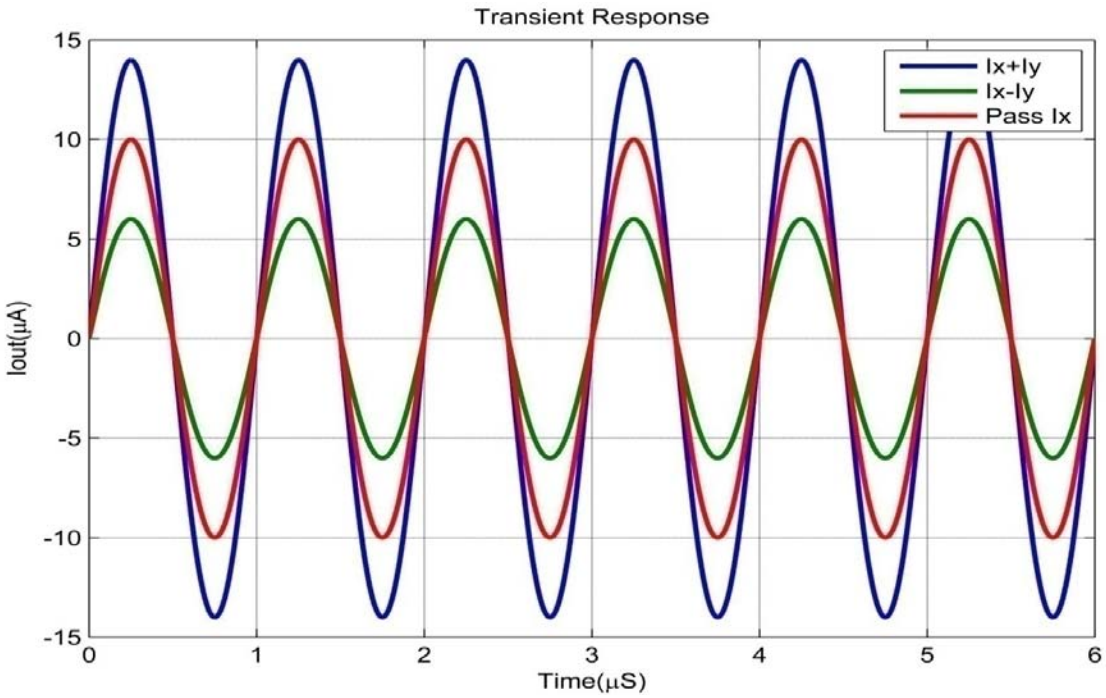


Figure 3.6 Transient response of A/S cell for addition, subtraction and pass

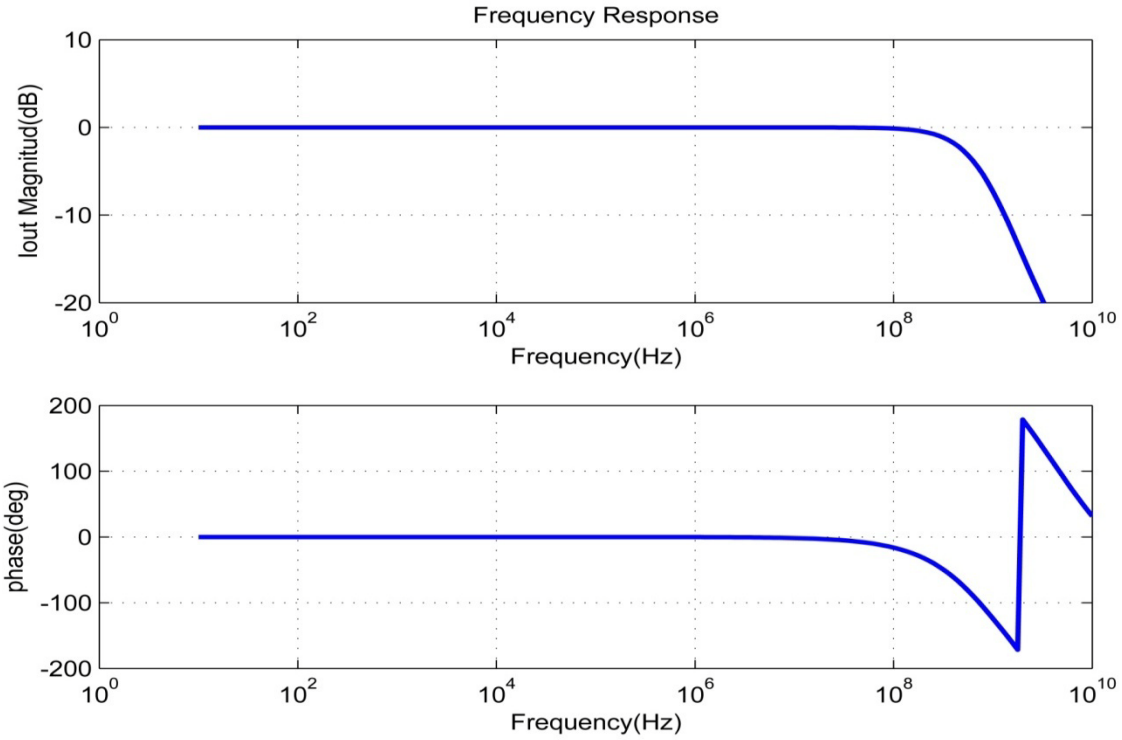


Figure 3.7 Frequency response of A/S cell

3.1.2 Integration – (INT) Cell

Switchless current mode integrators are highly recommended because the extensive use of switches and capacitors can severely degrade the frequency response of the circuit [32]. Several continuous time current mode integrators have been reported in the literature. One very attractive companding integrator for high frequency application is the one presented in [36]. However, its biggest disadvantage is that it is based on BJT transistors. Transistor level based strong inversion CMOS integrators found in the literature are mainly two types: square root domain companding integrators and current mirrors gm-C integrators.

The MOSFET companding integrators exploit the MOSFET trans-linear principles for compression and its square law characteristic for expansion. The square root domain companding integrator reported in [37] consists of two trans-linear blocks which are a square rooter and a multiplier divider in addition to some current mirrors.

The integrator presented in [38] is very similar in its idea to the one in [37], but it is using different geometric mean cell and two multiplier/divider cells instead of one. This design is immune to body effect in addition to the advantages of companding circuits.

Both integrators [37 and 38] have the advantage of large dynamic range, however, they are quite complex and their frequency performance is not investigated. Integrator [39] consists of two dividing circuits and one square root circuit. It also suffers from the complexity issue.

Current mirror $G_m - C$ integrators and their based filters are also common in the literature for example [40-47]. The basic component of this type of integrators are the

MOSFET trans-conductance and an additional capacitance. Almost all the mentioned circuits are realized by cascading two inverting current mirrors (amplifiers) with the output of the second stage fed back to the first stage. The additional capacitance is placed in parallel with the input node in order for the circuit to realize a $G_m - C$ block. These integrators can operate at relatively high frequency as in [43, 45 and 46]. In addition, fully differential version or inverting version can be easily made as in [42 and 43]. Moreover, they are capable of operation at low voltage and consumption of low power [42, 43, 45 and 47].

Due to the above advantages, current mirror based $G_m - C$ integrator is adopted, namely the one reported in [43]. The circuit proposed in [43] in its present form is not ready to be used in the integrator cell since it is not programmable or tunable. In addition, its starting frequency of operation is high (100 kHz) and needs to be extended lower than 100 kHz.

Figure (3.8) shows a slightly modified version of the inverting lossless integrator reported in [43]. The circuit in figure (3.8) and the circuit reported in [43] have the same structure but they differ in the value of the biasing current. This circuit consists mainly of two simple current mirrors, biasing currents and a capacitor C_1. The first current mirror is composed of transistors M1& $M2$ while the second current mirror is composed of M3 & $M4$. The small signal model of the circuit without the output conductance is shown in figure (3.9).

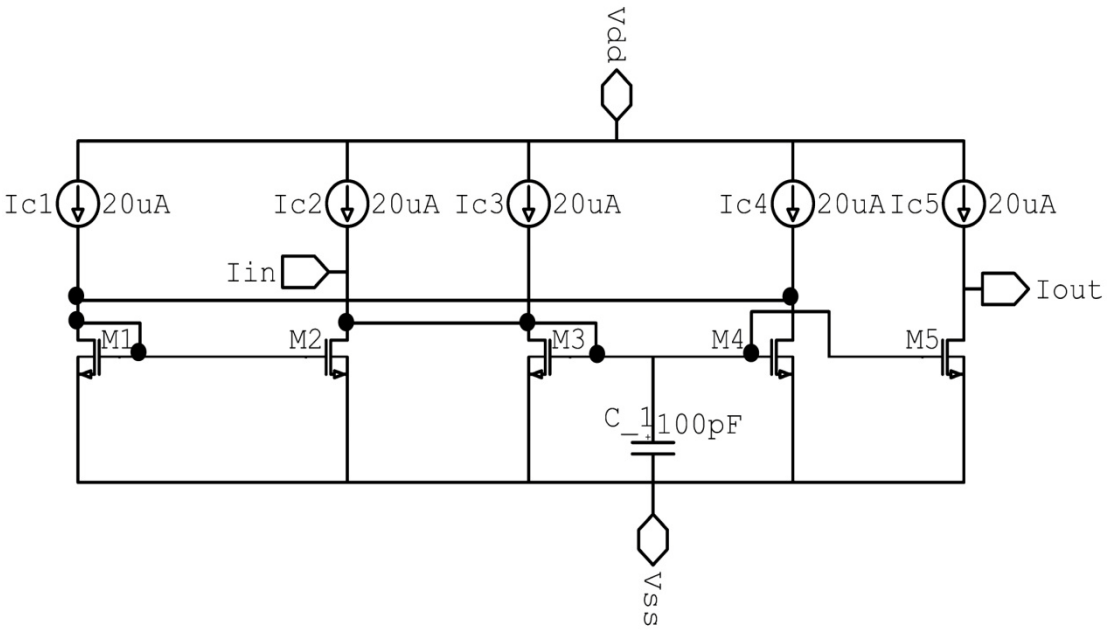


Figure 3.8 Inverting lossless integrator [43]

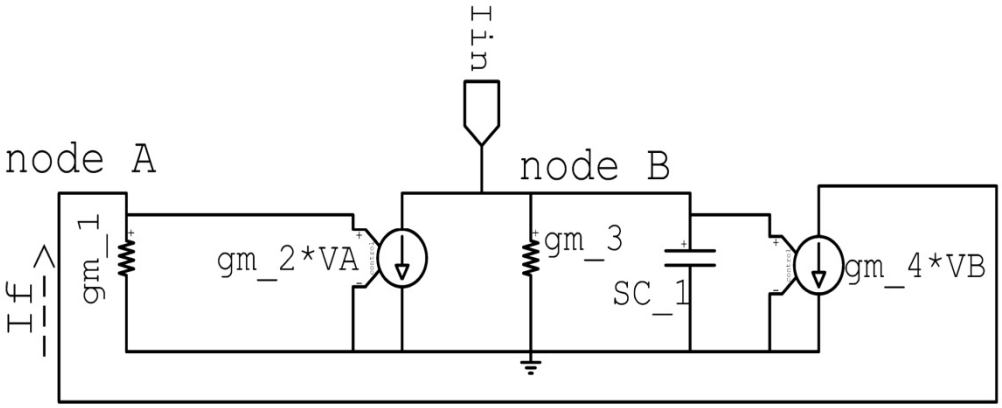


Figure 3.9 Integrator small signal model neglecting the output conductance

Based on this small signal model:

$$I_{in} = g_{m\_2} * V_A + \left(g_{m\_3} + SC\_1\right) * V_B \quad (3.1)$$

$$I_f = g_{m\_1} * V_A \quad (3.2)$$

$$I_f = -g_{m\_4} * V_B \quad (3.3)$$

Assuming that $g_{m\_1} = g_{m\_2}$ and $g_{m\_3} = g_{m\_4}$, substitution of equation (3.2 and 3.3) into equation (3.1) results in:

$$I_{in} = g_{m\_2} * \frac{I_f}{g_{m\_1}} + \left(g_{m\_3} + SC\_1\right) * \left(-\frac{I_f}{g_{m\_4}}\right) \quad (3.4)$$

$$I_f = \left(-g_{m\_3}/_{SC\_1}\right) * I_{in} \quad (3.5)$$

Since $I_f = I_{out}$, then:

$$\frac{I_{out}}{I_{in}} = -g_{m\_3}/_{SC\_1} = -A/_S \quad (3.6)$$

Equation (3.6) represents the transfer function of an inverting type lossless integrator. The integrator unity gin frequency is determined by $(A = \omega = g_m/_C)$ this factor depends on MOSFET trans-conductance which is:

$$g_m = \sqrt{2 * \mu_o * C_{ox} * W/_L * I_c} \quad (3.7)$$

Where μ_o is the electron mobility, C_{ox} is the capacitance per unit area of the gate oxide, $W/_L$ is the transistor aspect ratio and I_c is the biasing current. This means that tuning of the integrator unity gin frequency is possible if we are able to vary the biasing current I_c.

The control of the integrator unity gain frequency will be the key to have control over the cut off frequency of a filter.

In order to make the circuit in figure (3.8) suitable for use in the CAB, all biasing currents $I_{c1} - I_{c5}$ have to be programmable (ON or OFF) in order to determine the state of the integrator (ON or OFF), and tunable (vary in values) in order to determine the value of parameter (A) based on user's decision. These features will be integrated in the circuit in section 3.2 and 3.3 of this report.

Simulation results of the circuit in figure (3.8) are reported in this section. These results are obtained at the following circuit parameters: transistors aspect ratio $W/L = 10\mu/1\mu$, all biasing currents $I_{c1} - I_{c5} = 20\mu A$, V_{dd} & $V_{ss} = \pm 1.5V$, Capacitor $C_1 = 100pF$, $R_{Load} = 1k\Omega$.

The power consumption of the circuit is around 87 µW. Figure (3.10) shows the phase and magnitude frequency response of the integrator which indicate that it can work well starting from 20 kHz up to the range of few GHz.However, the phase response deviate at the start and end of the frequency range creating some phase error. Figure (3.11) shows the transient response of the integrator when injected with an input current of amplitude 10µA and frequency 500 KHz.

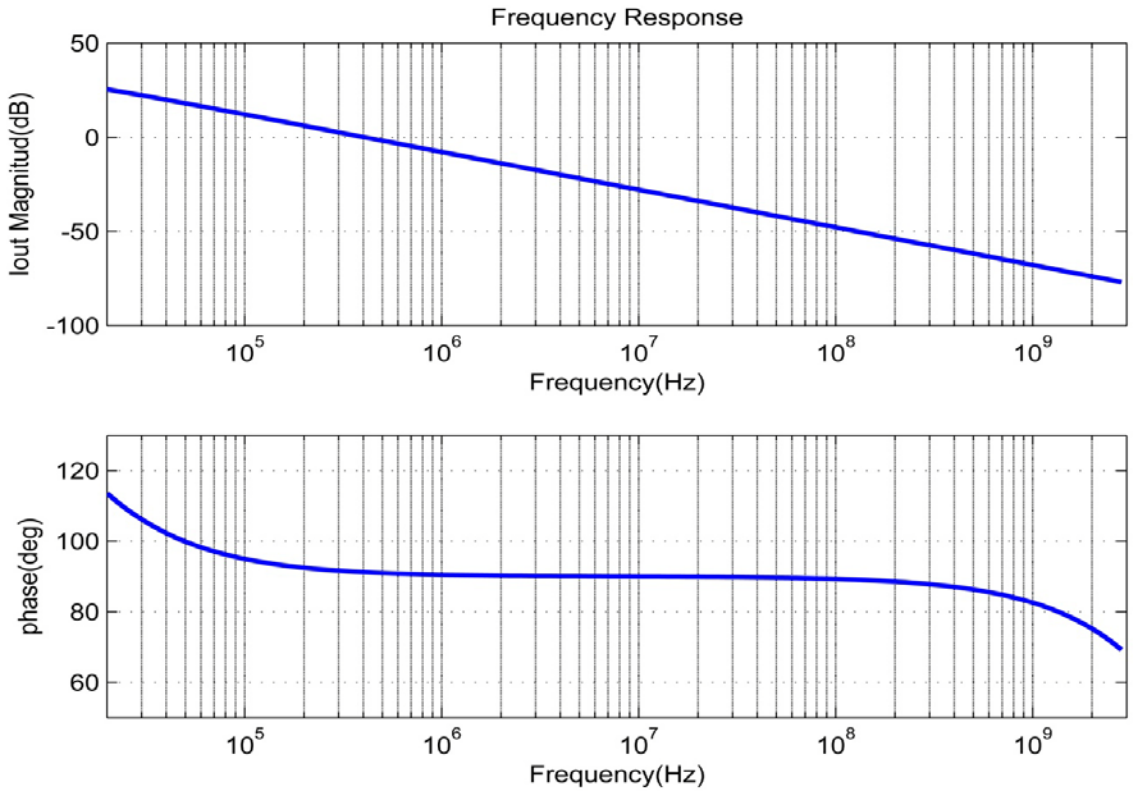


Figure 3.10 Integrator frequency response

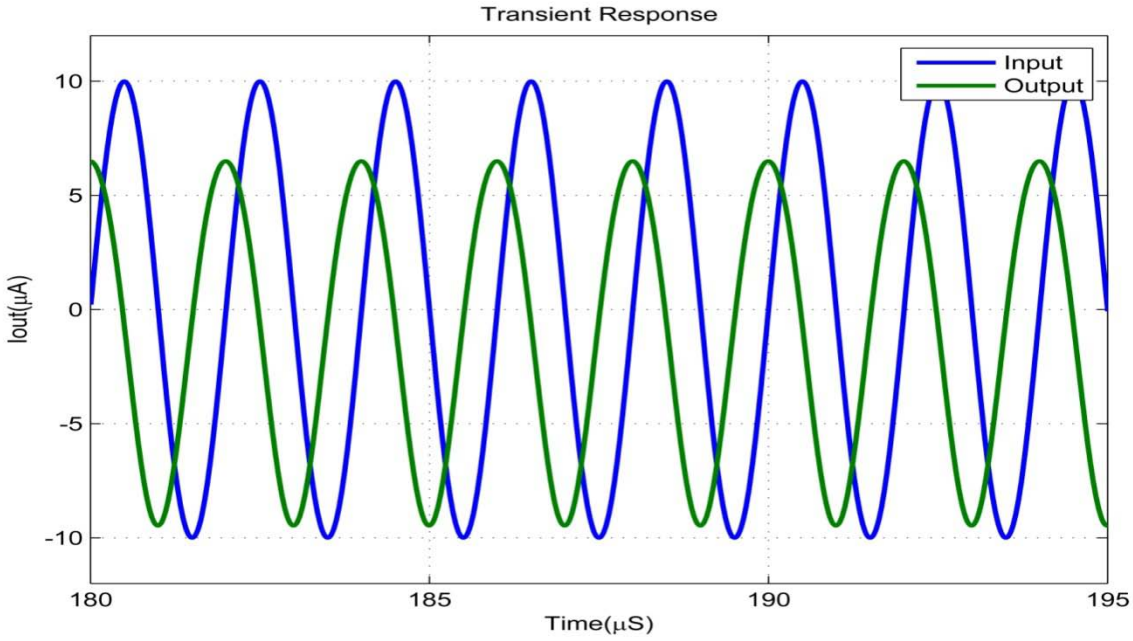


Figure 3.11 Integrator transient response

The aimed integration cell is capable of performing either integration or pass of the input current. Therefore, in order to form the complete integration cell, the integration circuit will be occupied with a bypass switch at the input node in addition to the controllable biasing currents.

3.1.3 Multiplication/Division – (M/D) Cell

The multiplication/Division functions are very fundamental in analog signal processing. Therefore, a multiplier circuit constitutes a basic block in many applications such as modulation, demodulation, rectification, amplification and automatic gain controlling. This justifies the growing interest in developing this circuit proven by the large number of publications in this area, see references [48-58].

Most of the reported current mode continuous time multipliers fall in different category of circuits such as : trans-linear principle of MOSFET in sub-threshold or in saturation [48,49,53-56], square root and squarer circuits based on square low of MOSFET in saturation [57] and class AB circuits [50,58]. The different designs depend on the basic principle of design which is the square-difference identity in most publications. As a result, a squarer cell and a subtractor cell are found in many designs of multiplier circuits. The design reported in [49] uses a quite simple architecture, but it requires large power supply of $\pm 3V$ which will make its power consumption very high. In addition, the achieved BW is relatively small(10.7MHz). This multipier is used in very attractive and non-traditional application which is a phase detector. The multiplier reported in [50] is class AB and based on MOSFET dual translinear loops in addition to current mirrors. The interesting point about this multiplier is that it can be used as current multiplier, voltage multiplier or current and voltage multiplier. The main drawback of this multiplier

is that it could not achieve a BW higher than 19MHz . Another interesting multiplier is reported in [51]. It is based on MOSFET square low characteristic. Even though, this multiplier achieves a bit higher BW than [49 and 50], it requires large power supply of +5Vwhich results in high power consumption(930μW).

Recently, a multiplier/divider circuit with acceptable features is reported in [48] and shown in figure (3.12). This circuit is based on dual trans-linear loops of MOSFET transistors operating in saturation. It is reported to achieve BW of 41.8MHZ and power consumption of 340μW. However, the circuit needs some modifications in order to be suitable for use in the CAB. Its achieved BW will be enhanced to a value larger than what is reported. In addition, one of its nodes is an input and output node at the same time which creates a conflict of interest, so this problem needs to be solved. Additionally, in different section of this report, switching capability will be added to the circuit via bypassing one of its inputs current through a switch.

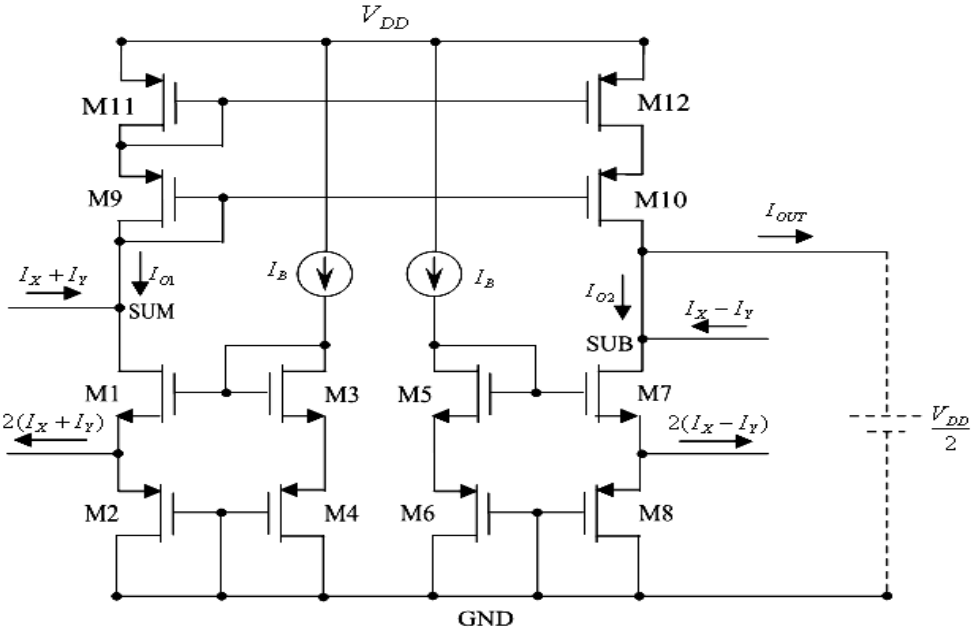


Figure 3.12 Analog multiplier/divider reported in [48]

Figure (3.13) represent the basic circuit structure of the proposed multiplication/division circuit. Its structure is based on the trans-linear loop shown in figure (3.14).

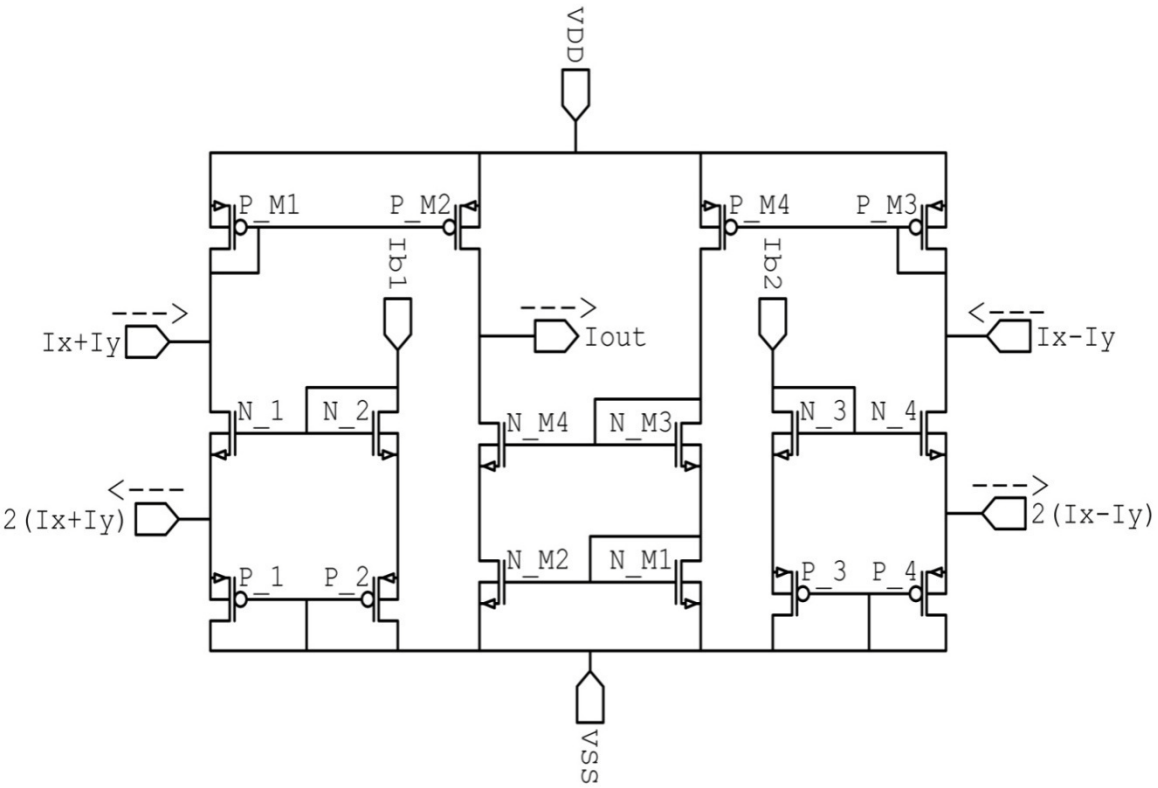


Figure 3.13 Proposed basic multiplier/divider Circuit

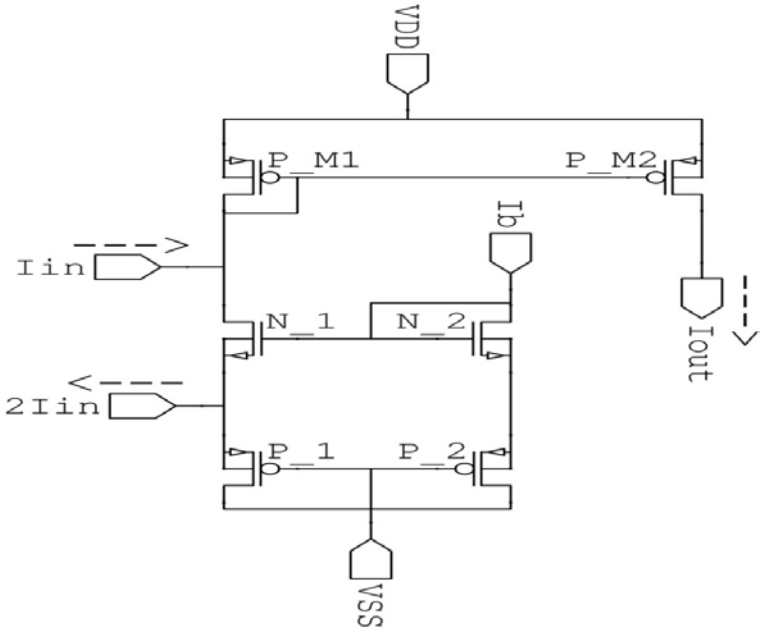


Figure 3.14 Trans-linear loop for the multiplier/divider circuit

The trans-linear loop consists of transistors $N\_1, N\_2, P\_1 \& P\_2$; all are biased in saturation region. The relationship between the drain current (I_{DS}) and the gate to source voltage (V_{GS}) of a transistor operating in saturation is given by:

$$I_{DS} = K(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{3.8}$$

Assuming that the effect of λ is negligible:

$$V_{GS} = V_{th} + \sqrt{\frac{I_{DS}}{K}} \tag{3.9}$$

Where V_{th} is the threshold voltage, $K = 0.5\mu_o C_{ox}(\frac{W}{L})$ is the trans-conductance parameter of the transistor, μ_o is electron mobility, C_{ox} is the oxide gate capacitor, $\frac{W}{L}$ is the transistor aspect ratio, λ is the channel length modulation parameter and V_{DS} is the drain to source voltage . By using KVL in the trans-linear loop gives:

$$V_{GS(P\_1)} + V_{GS(N\_1)} = V_{GS(P\_2)} + V_{GS(N\_2)} \tag{3.10}$$

Assuming the four transistors are matched and biased in saturation, and considering that

$$I_{DS(N\_2)} = I_{DS(P\_2)} = I_b \tag{3.11}$$

Where I_b is the bias current, then combining equation (3.9) and (3.10) yields:

$$\sqrt{I_{DS(P_1)}} + \sqrt{I_{DS(N_1)}} = \sqrt{I_{DS(P_2)}} + \sqrt{I_{DS(N_2)}} \tag{3.12}$$

$$\sqrt{I_{DS(P_1)}} + \sqrt{I_{DS(N_1)}} = 2\sqrt{I_b} \tag{3.13}$$

In order to find the relation between I_{in} & I_{out}, KCL equations at the source and at the drain of transistor N_1 will be written:

$$I_{DS(N_1)} = I_{in} + I_{out} \tag{3.14}$$

$$I_{DS(P_1)} = I_{out} - I_{in} \tag{3.15}$$

Now, by substituting (3.14) & (3.15) into (3.13) and squaring both sides:

$$4I_b = (I_{in} + I_{out}) + (I_{out} - I_{in}) + 2\sqrt{{I_{out}}^2 - {I_{in}}^2} \tag{3.16}$$

$$4I_b - 2I_{out} = 2\sqrt{{I_{out}}^2 - {I_{in}}^2} \tag{3.17}$$

$${16I_b}^2 - 16I_B I_{out} + 4{I_{out}}^2 = 4({I_{out}}^2 - {I_{in}}^2) \tag{3.18}$$

Then the output current of figure (1.14) can be written as:

$$I_{out} = \frac{{I_{in}}^2}{4I_b} + I_b \tag{3.19}$$

It is clear from equation (3.19) that the circuit in figure (1.14) represents a current squarer function. This squarer cell will be the basic building block in the analog multiplier/divider. The principle of operation of the designed multiplier is based on the following square difference identity:

$$(x + y)^2 - (x - y)^2 = 4xy \tag{3.20}$$

The proposed multiplier/divider in figure (3.13) contains two squaring cells and current mirrors. Transistors $N\_1, N\_2, P\_1 \& P\_2$ constitute the first squarer with input $(I_x + I_y)$. The resulting output through transistor P_M1 and P_M2 is given by:

$$I_{out\,1} = \frac{(I_x + I_y)^2}{4I_{b1}} + I_{b1} \tag{3.21}$$

The other squarer is composed of transistors $N\_3, N\_4, P\_3 \& P\_4$ with input $(I_x - I_y)$. The resulting output through transistor P_M3 and P_M4 is given by:

$$I_{out\,2} = \frac{(I_x - I_y)^2}{4I_{b2}} + I_{b2} \tag{3.22}$$

The resulting output (I_{out}) of the multiplier is the subtraction of $I_{out\,1}$ and the mirror of $I_{out\,2}$ through transistors N_M1 to N_M4 :

$$I_{out} = I_{out\,1} - I_{out\,2} \tag{3.23}$$

$$I_{out} = \frac{(I_x + I_y)^2}{4I_{b1}} + I_{b1} - \frac{(I_x - I_y)^2}{4I_{b2}} - I_{b2} \tag{3.24}$$

Since $I_{b1} = I_{b2} = I_b$ (constant biasing current) , then:

$$I_{out} = \frac{I_x I_y}{I_b} \tag{3.25}$$

From equation (3.25) it is obvious that the proposed circuit functions as multiplication of two signals (I_x& I_y) and division by (I_b) .Since the input output relation of this multiplier involves I_b in the denominator, the circuit can be used as a divider. By keeping the current I_x (or I_y) constant, the output current will be proportional to I_x/I_b (or I_y/I_b) and thus a divider function is obtained. However, care must be taken since (I_b) is the biasing current, it can be varied only to limited extent.

One advantage of this circuit over the one reported in [48], is that it can operate at higher frequencies due to the reduction of the parasitic capacitance generated by the cascade current mirror used. Another addition to this circuit is that the output node is distinct from the input nodes. The circuit reported in [48] has the node ($I_x - I_y$), high impedance node ($2 * r_{\circ_{(N\_4)}}$) as both input and output node at the same time. However, in the proposed circuit of figure (3.13) the two nodes are separated so that the input node for ($I_x - I_y$) is at low impedance and the output node for (Iout) is at high impedance.

Approximate impedances at all concerned nodes are listed below:

- Input impedance at $(I_x + I_y)$ node:

$$\frac{1}{g_{m_{(P\_M1)}}} // \left[r_{\circ_{(N_1)}} \left(1 + g_{m_{(N\_1)}} \left(\frac{1}{g_{m_{(P\_1)}}}\right)\right)\right] \approx \frac{1}{g_{m_{(P\_m1)}}} \tag{3.26}$$

- Input impedance at $2(I_x + I_y)$ node:

$$\frac{1}{g_{m_{(P\_1)}}} // \left[\frac{1}{g_{m_{(N\_1)}}} \left(1 + \frac{1}{r_{\circ_{(N\_1)}} * g_{m_{(P\_M1)}}}\right)\right] \approx \frac{1}{2g_{m_{(P\_1)}}} \tag{3.27}$$

- Input Impedance at $(I_x - I_y)$ node:

$$\frac{1}{g_{m_{(P\_M3)}}} // \left[r_{\circ_{(N\_4)}} \left(1 + g_{m_{(N\_4)}} \left(\frac{1}{g_{m_{(P\_4)}}}\right)\right)\right] \approx \frac{1}{g_{m_{(P\_M3)}}} \tag{3.28}$$

- Input Impedance at $2(I_x - I_y)$ node:

$$\frac{1}{g_{m_{(P\_4)}}} // \left[\frac{1}{g_{m_{(N\_4)}}} \left(1 + \frac{1}{r_{\circ_{(N\_4)}} * g_{m_{(P\_M3)}}}\right)\right] \approx \frac{1}{2g_{m_{(P\_4)}}} \tag{3.29}$$

- Output impedance at (I_{out}) node:

$$r_{\circ_{(P\_M2)}} // \left[r_{\circ_{(N\_M4)}} \left(1 + g_{m_{(N\_M4)}} r_{\circ_{(N\_M2)}}\right)\right] \approx r_{\circ_{(P\_M2)}} \tag{3.30}$$

Where in all above equations $r_{\circ_x}$ and g_{m_x} are the output resistance and trans-conductance of transistor x respectively.

Simulation of the proposed multiplier/divider is carried out based on the following circuit parameters: V_{DD} & $V_{SS} = \pm 1.5$ V, bias current $I_b = 10\mu A$, the output port is connected to a load resistance $R_{Load} = 1k\Omega$. The aspect ratio of transistors used is presented in table (4).

Table 4 Transistors aspect ratio of the proposed multiplier/divider

Device	N_1 to N_4	N_M1 to N_M4	P_M1 to P_M4	P_1 to P_4
W/L(μ/μ)	1/0.6	1.7/0.5	2.02/1	2.23/0.4

Figure (3.15) shows the DC transfer characteristic of the proposed multiplier/divider when both inputs (I_x & I_y) are varied between $-10\mu A$ & $10\mu A$. The results from the figure agree well with the theory. It shows that the circuit operates correctly as a four quadrant multiplier. The Linearity error of the proposed circuit is around 1.6% and the power consumption is about 158 μW.

Figure (3.16) shows the transient operation of the multiplier having both inputs (I_x & I_y) as sinusoidal signals at 1MHz with two differet amplitudes.

The frequency response of the proposed multiplier/divider is presented in figure (3.17). The -3dB bandwidth of the circuit is about 440MHz. This high bandwidth achieved by the circuit is due to the reduction of high values of parasitic capacitance generated by the cascade mirror in the circuit of figure (3.12).

The use of the circuit as a divider of two currents is shown in figure (3.18) in which I_b & I_y are varied, while I_x is kept fixed at$10\mu A$.

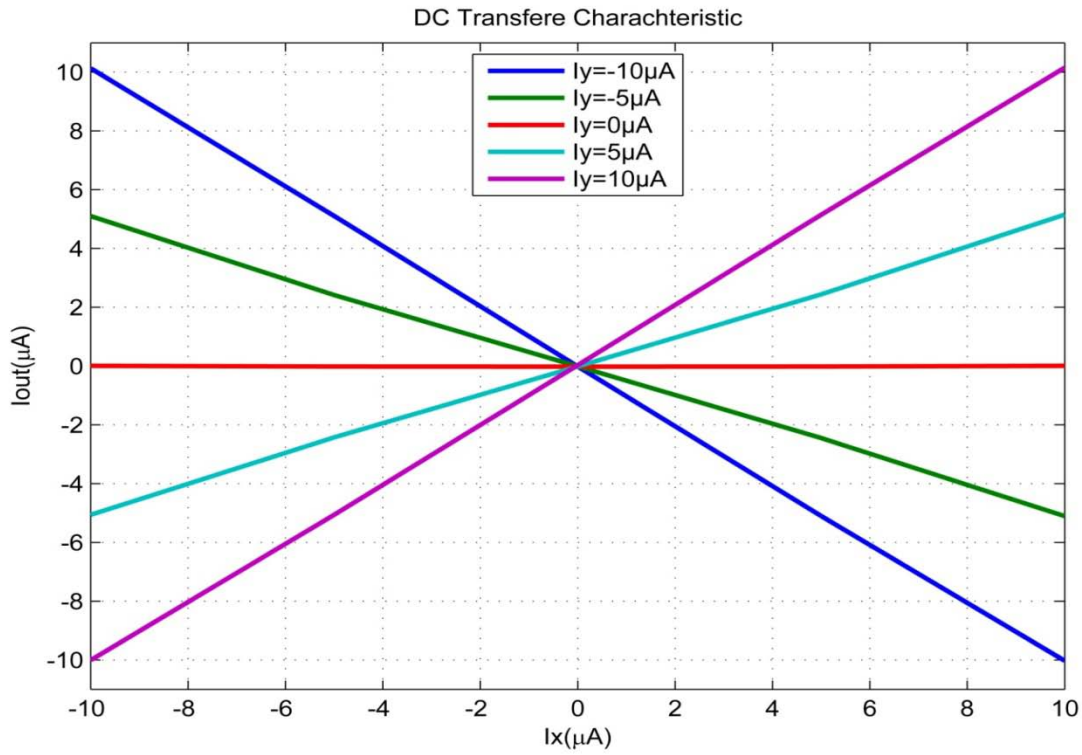


Figure 3.15 DC transfer characteristic of the proposed multiplier/divider

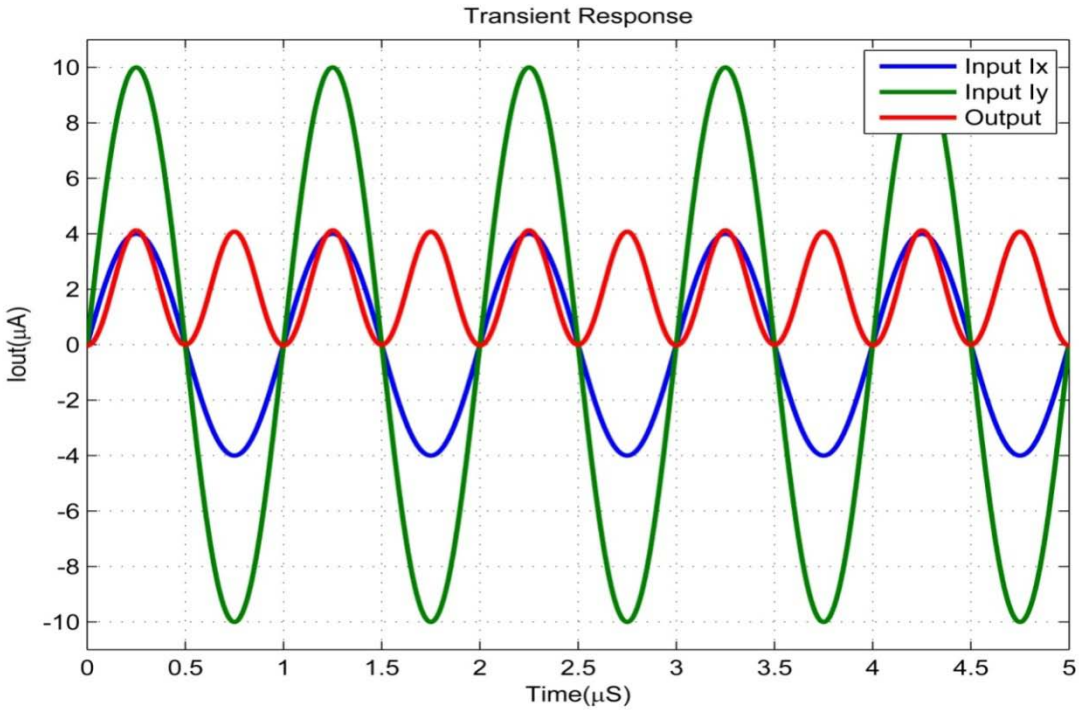


Figure 3.16 Transient response of the proposed multiplier/divider

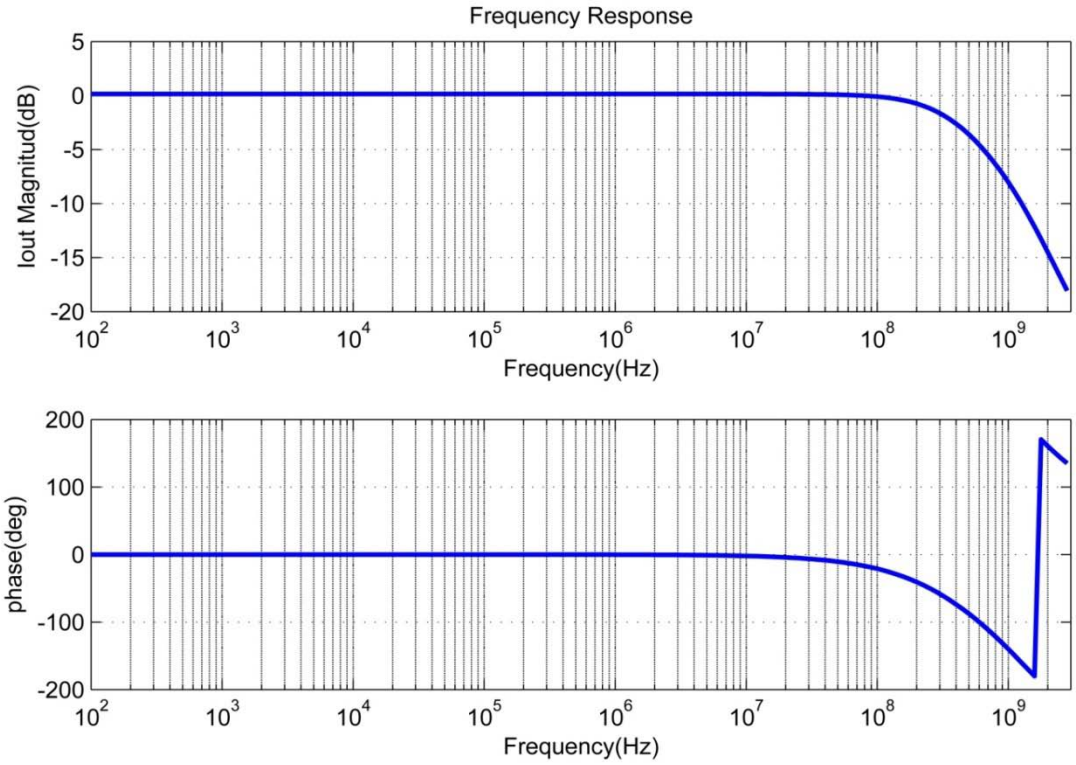


Figure 3.17 Frequency response of the proposed multiplier/divider

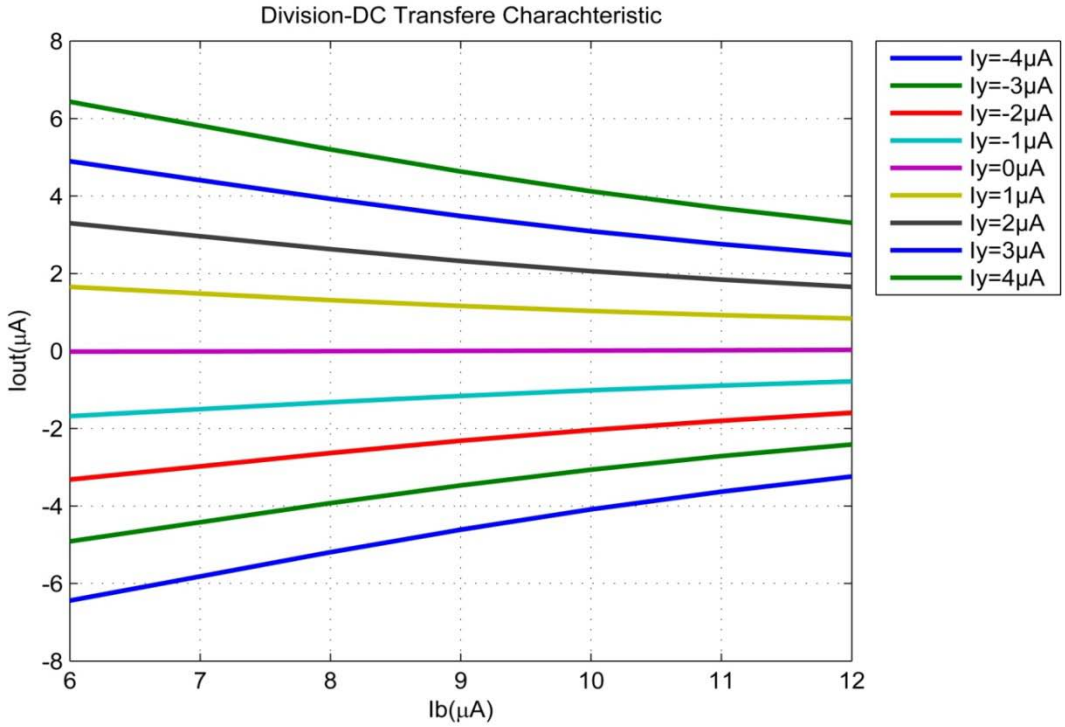


Figure 3.18 DC characteristic of the proposed multiplier working as a divider,

Ix =10uA

Comparison of the key performance parameters between the proposed multiplier/divider and previously reported works is shown in table (5).It is clear that the proposed circuit is better in many aspects such as bandwidth and power consumption and area.

Table 5 Comparison between proposed multiplier/divider and previous works

Features	**Proposed**	**Ref.[48]**	**Ref.[49]**	**Ref.[50]**	**Ref.[51]**
Power Supply	$\pm$1.5 V	+3.3 V	$\pm$3V	$\pm$1.5 V	+ 5V
Linearity Error	1.6%	1.1%	-	1.2%	1.22%
Bandwidth	440 MHz	41.8 MHz	10.7 MHz	19 MHz	22.4 MHz
Power	158 µW	340 µW	-	460 µW	930 µW
Technology	0.35 µm	0.35µm	2 µm	0.5 µm	2 µm
Approximate Area (mm^2)	0.0054	-	0.57	0.161	0.144

Since the proposed circuit is designed to work as four quadrant multiplier of two inputs I_x & I_y following this equation: $I_{out} = \frac{I_x I_y}{I_b}$ where I_b is the biasing current. From the equation, it is clear that switching either of the two inputs off will result in zero output. On the other hand switching the bias current off will not do this job. Therefore, for a complete multiplier/divider cell to be designed, this circuit is controlled either to be a multiplier/divider or a pass cell using dual switches at the input I_x.

3.2 Biasing – Programming Sources and Switches

In most of the reported CAB designs, the programmability and tunability were achieved using banks of programmable resistors, capacitors and switches resulting in limited bandwidth and large silicon area [5]. Other reported designs use floating gate transistors. However, their main drawback is that they do not use the standard CMOS process. To avoid using programmable resistors, capacitors, switches, and FG transistors, the method of digitally modifying the biasing currents which does not degrade the signal frequency is used. Sometimes it is also required to use switches, so, their use is restricted to certain places.

The biasing sources of the circuits in figure (3.1) and (3.8) have to be controllable by digital bits, such that they are either ON (at $20\mu A$) or OFF ($at\ 0\mu A$). A possible realization of such current sources is reported in [32 and 59].

3.2.1 Biasing and Programming of Adder-Subtractor Circuit

The circuit in figure (3.19) is the one used in reference [32] for biasing and programming. A slightly modified circuit, from the one presented in [32], to fit our needs is shown in figure (3.20). This circuit is used to bias the adder-subtractor circuit previously shown in figure (3.1). This circuit generates three equal copies of current $I_{s1} = I_{s2} = I_{s3} = 20\mu A$. The value of this current depends on the voltage difference between the gate and the source of transistor P_c. The gate of this transistor controls the output currents and make them either ON or OFF via S_Sub. This signal (S_Sub) is part of the control word of the CAB, as it can control the addition operation, and it should be coming from the output of a D-Latch. The source of transistor $P - c$ is connected to a reference voltage $Vctrl\_as$

adjusted to assure that the currents $I_{s1} - I_{s3}$ are always at $20\mu A$ in the ON state. The generated current is mirrored through transistors $N-1\ to\ N-4\ and\ P-1\ to\ P-8$ in order to generate the required copies. These three copies are used to bias the three subtraction branches in the circuit of figure (3.1). The circuit in figure (3.21) is the same as the one presented in figure (3.20), except that the input at the gate of transistor $P-c$ is S_Adder since it is to be used to bias the addition branches of circuit (3.1). The transistor aspect ratio of figure (3.20) used are ${}^{2\mu}/_{1\mu}$ for transistor $P-c$, ${}^{5\mu}/_{1\mu}$ for transistors $N-1\ to\ N-4$ and ${}^{20\mu}/_{1\mu}\ for\ P-1\ to\ P-8$ with $V\ ctrl\_as = 276mV$.

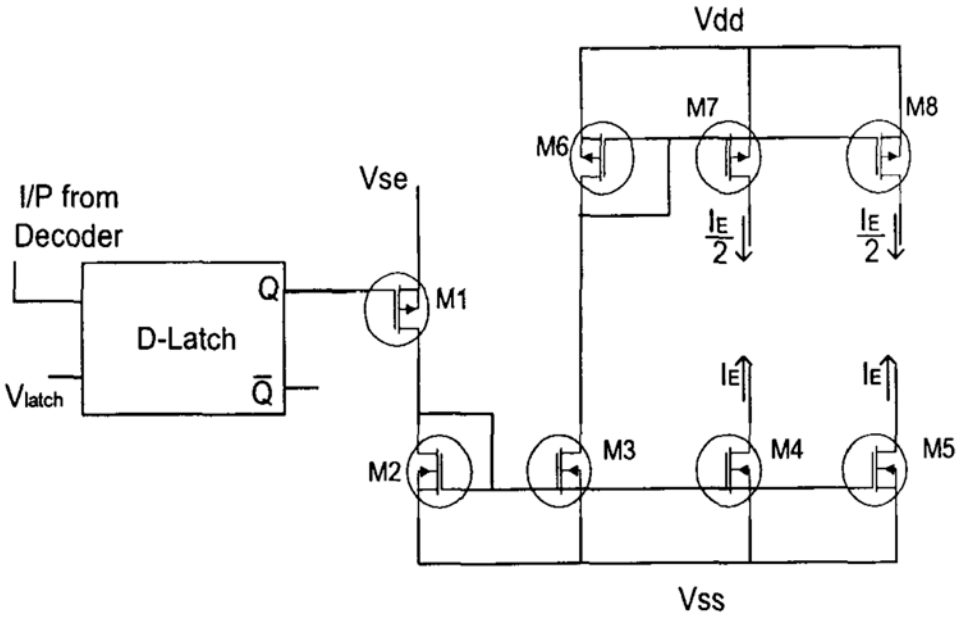


Figure 3.19 Biasing and programming circuit used in ref. [32]

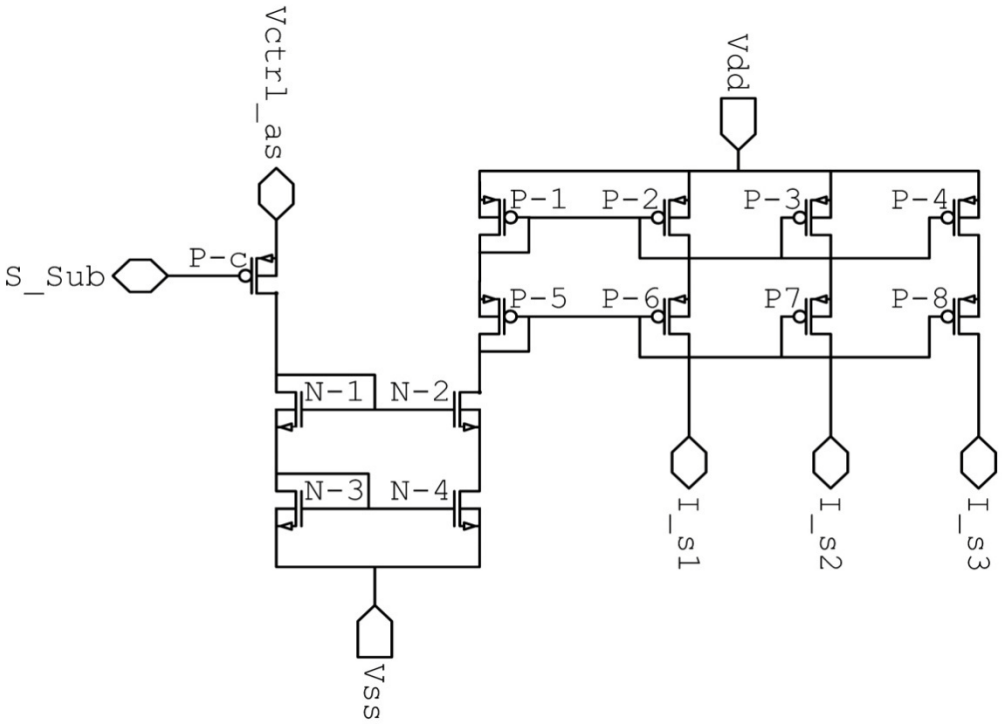


Figure 3.20 Biasing-programming circuit for subtraction

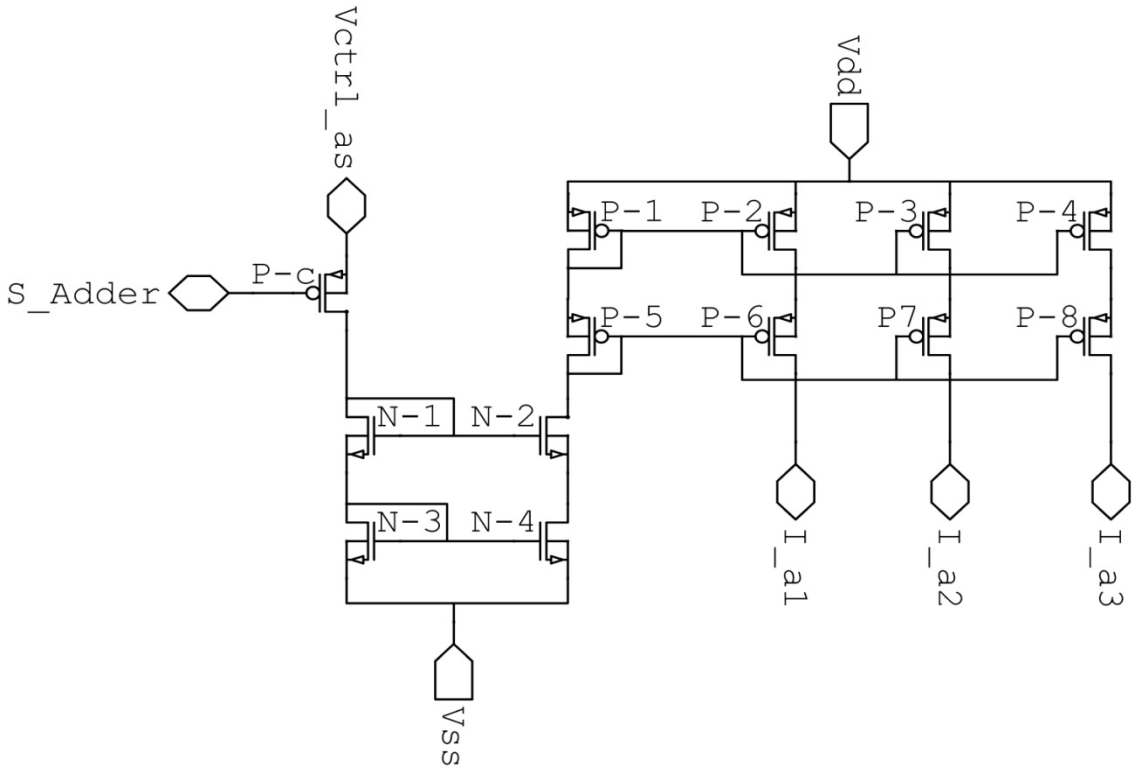


Figure 3.21 Biasing-programming circuit for addition

3.2.2 Biasing and Programming of Integrator Circuit

Figure (3.22) shows a circuit used in biasing the integrator circuit of figure (3.8) similar to the one presented in figure (3.20). This biasing circuit generates five equal copies $I_{c1} = I_{c2} = I_{c3} = I_{c4} = I_{c5} = 20\mu A$. The gate of transistor $P - c$ is controlled by SC_I which controls the currents $I_{c1} - I_{c5}$ and makes them either ON or OFF which in turns controls the integrator circuit. SC_I is the complement of S_I which is part of the control word bits. SC_I should be coming from a D-latch to the gate of $P - c$. The aspect ratio of transistors and $Vctrl\_i$ is the same vales used for the circuit in (3.20)

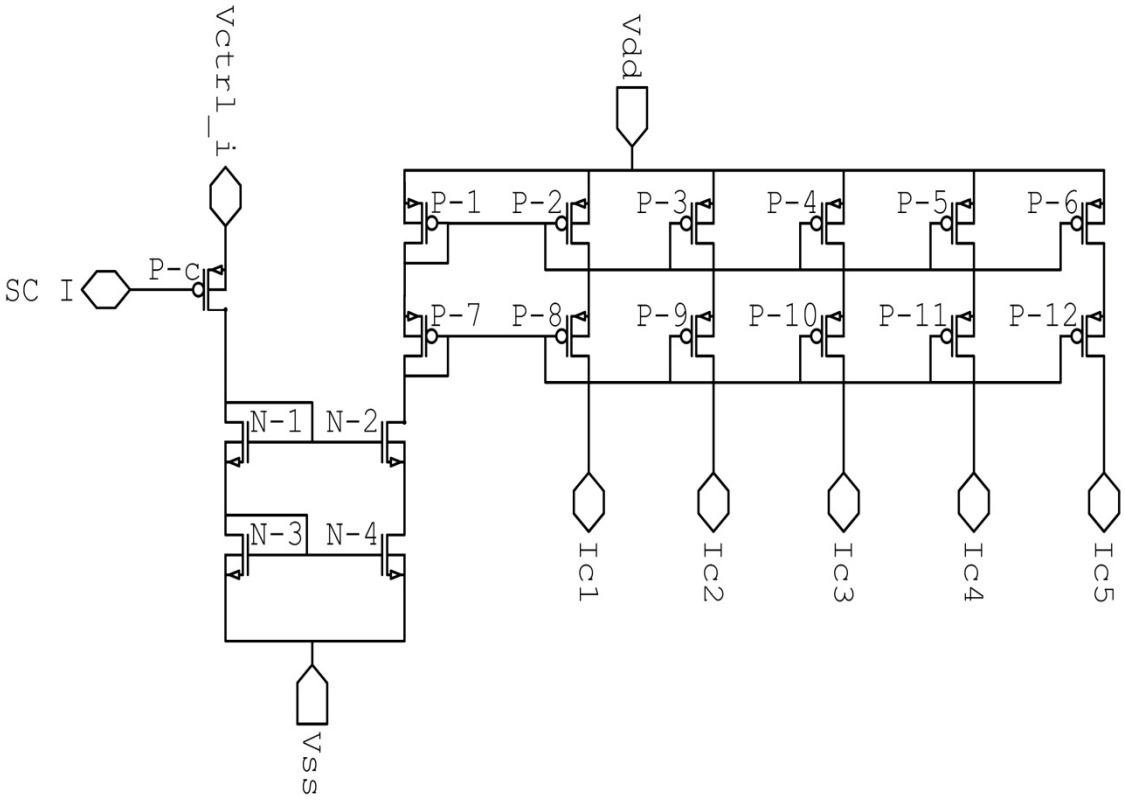


Figure 3.22 Biasing-programming circuit for integrator

3.2.3 Biasing of Multiplier/Divider Circuit

Figure (3.23) presents the biasing circuit utilized to bias the proposed multiplier/divider of figure (3.13). It generates two biasing currents $I_{b1} = I_{b2} = 10\mu A$. It functions in similar way to the circuit in figure (3.20) except that transistor P_c is removed since control over these biasing currents is not needed in the multiplier/divider. This is because switching off the biasing current will not help in making the multiplier/divider in its OFF state since it is in the denominator of ($I_{out} = \frac{I_x * I_y}{I_b}$). The transistors aspect ratio used in figure (3.23) is ${}^{1\mu}/_{1\mu}$ for N-1 to N-4 and ${}^{20\mu}/_{1\mu}$ for P-1 to P-6 with $Vctrl\_m = 284mV$.

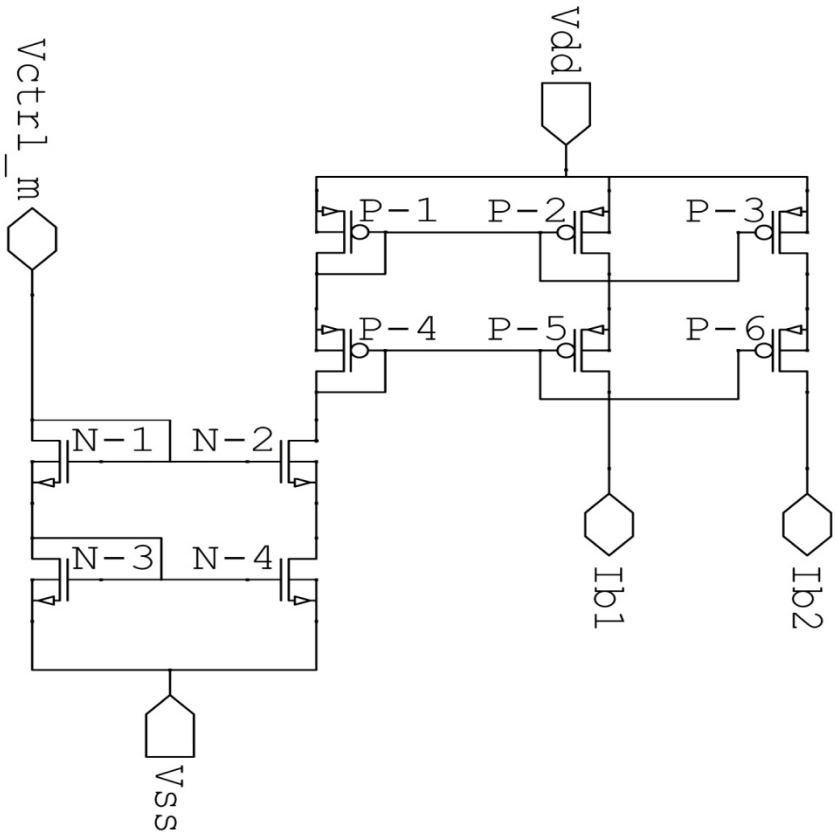


Figure 3.23 Biasing circuit for the multiplier/divider

3.2.4 Programming Switches

In addition to the controllable bias currents and their use in configuring the CAB function, switches are also used but to a limited extent. Two types of switches are use: bypass switch and blocking switch. Figure (3.24) shows the bypass switch used at the input of the integrator. Its function is either to allow the input to enter the integrator through transistor N_B or to bypass it to the integrator output, when it is in the OFF state, through transistor N_A. This operation is determined by the control bit S_I and its complement. Aspect ratio of the transistors used is $^{5\mu}/_{1\mu}$ for N_B and $^{12\mu}/_{0.5\mu}$ for N_A. Similar bypass transistor are also used at the input (I_x) of the multiplier/divider. Its function is determined by the control bit S_M and its complement as shown in figure (3.25). Aspect ratio of the transistors used is: $^{3\mu}/_{1\mu}\ for\ N\_B$ and $^{10\mu}/_{0.5\mu}\ for\ N\_A$.

The blocking switch in figure (3.26) is used at the output of the multiplier/divider. It allows the output current only in one direction (out of the multiplier). So, it is either to bypass any current from the multiplier/divider to ground through N_B or it allows it to the next stage if it is in the ON state. As a result, currents entering the multiplier/divider at the output from any stage are not allowed. Aspect ratio of the transistors used is $^{2.5\mu}/_{1\mu}\ for\ N\_B$ and $^{10\mu}/_{0.5\mu}\ for\ N\_A$.

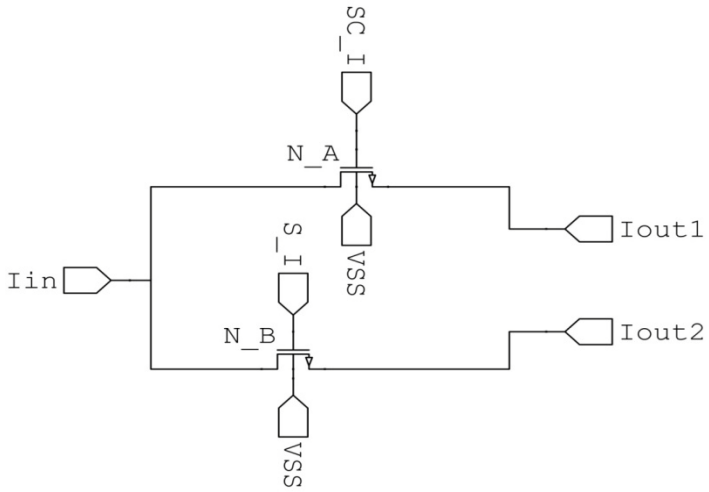


Figure 3.24 Bypass switch for the integrator

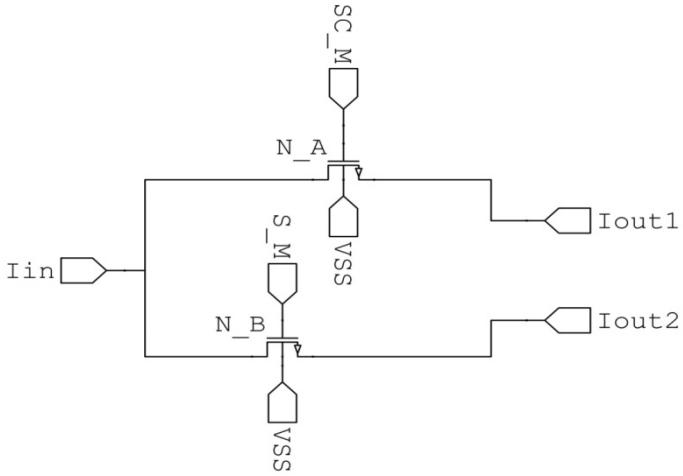


Figure 3.25 Bypass switch for the multiplier/divider

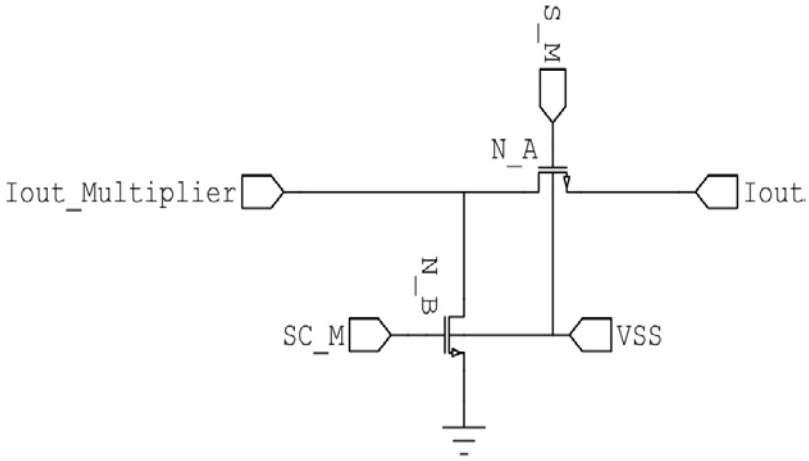


Figure 3.26 Blocking switch for the multiplier/divider

From the above programming currents and switches, part of the control word of the CAB can be determined. The programming of the CAB consists of four digits which are responsible for selecting the function to be achieved. These four digits, as per table (6), are sufficient to cover all the functions. Table (6) shows part of the control word (bits) which can select the mode of operation of the CAB.

Table 6 Programming bits for function selection

$B3$ S_M	$B2$ S_I	$B1$ S_Sub	$B0$ S_Adder	Function
0	0	1	1	Pass
0	0	1	0	Addition
0	0	0	1	Subtraction
0	1	1	1	Integration
1	0	1	1	Multiplication/Division

3.3 Supplementary Circuits

In order to facilitate the investigation of the performance of the CAB when configured into an FPAA, some additional circuits need to be built such as current mirrors and digitally programmable tuning currents.

3.3.1 Digitally Programmable Tuning Currents

In order for the integrator circuit tunability of parameters to be achieved, the digitally programmable currents in figure (3.27) and figure (3.28) are used [32]. The circuit in figure (3.27) is used for biasing current coarse tuning. It consists of the digitally programmable currents generated by transistors $PMOS\_1 - PMOS\_7$ and the current mirrors realized by transistors $N\_1 - N\_4\ and\ P\_1 - P\_12$. The W/L of transistors $PMOS\_1 - PMOS\_7$ are all the same and all are working in saturation. The generated current originates from three units; each is responsible of generating current component proportional to the number of MOSFETs forming it. These three units are:$PMOS\_1$ generating current I_o, $PMOS\_2$ & $PMOS\_3$ generating current $I_1$and $PMOS\_4 - PMOS\_7$ generating current I_2. The gates of each unit are connected to three signals $D_0, D_1\ and\ D_2$ respectively. These signals represent data bits which are part of the control word of the CAB. The sources of all thee seven transistors are connected to a reference voltage $Vctrl\_i\_ct$ which is adjusted to avalue of $875mV$ in order to make the value of $I_o = 10\mu A$. It should be noted that $I_2 = 2I_1 = 4I_o$. So, based on the values of $D_O - D_2$, the coarse tuning circuit can generate a current ranging from $0\mu A\ to\ 70\mu A$ in increment of $10\mu A$. In addition, this circuit can be extended to generate higher values of current if required. The generated current is mirrored and the required five copies are generated

I_{ct_1} to I_{ct_5} which are added to the integrator biasing. The aspect ratios are presented in table (7).

Table 7 Transistors aspect ratio for integrator coarse tuning circuit

Transistor	W	L
$PMOS\_1$ to $PMOS\_7$	1μ	5μ
Remaining transistors	20μ	0.5μ

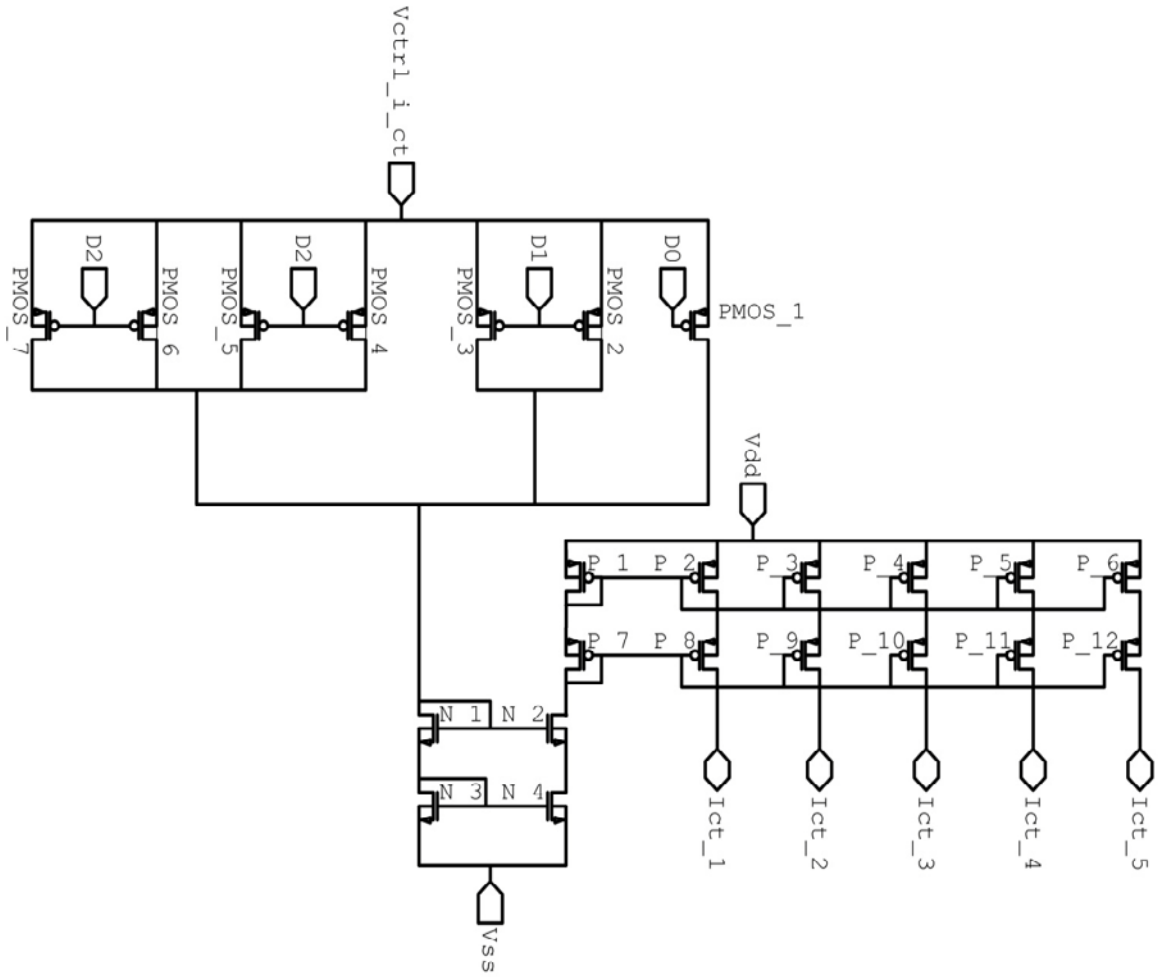


Figure 3.27 Digitally programmable coarse tuning current for the integrator

Figure (3.28) circuit is used as fine tuning for the integrator biasing. The three signals controlling the generated current are: D_3, D_4 and D_5 which also depend on digital bits

from the control word. The reference voltage $Vctrl\_i\_ft$ is adjusted to a value of $670mV$ in order to mak the current generated by $PMOS\_1$, $I_3 = 1\mu A$. So, based on the values of $D_3 - D_5$, the fine tuning circuit can generate a current ranging from $0\mu A\ to\ 7\mu A$ in increment of $1\mu A$. The required five copies are generated$I_{ft_1}\ to\ I_{ft_5}$. The aspect ratios used are shown in table (8).

Table 8 Transistors aspect ratio for integrator fine tuning circuit

Transistor	W	L
$PMOS\_1\ to\ PMOS\_7$	0.5μ	20μ
Remaining transistors	20μ	0.5μ

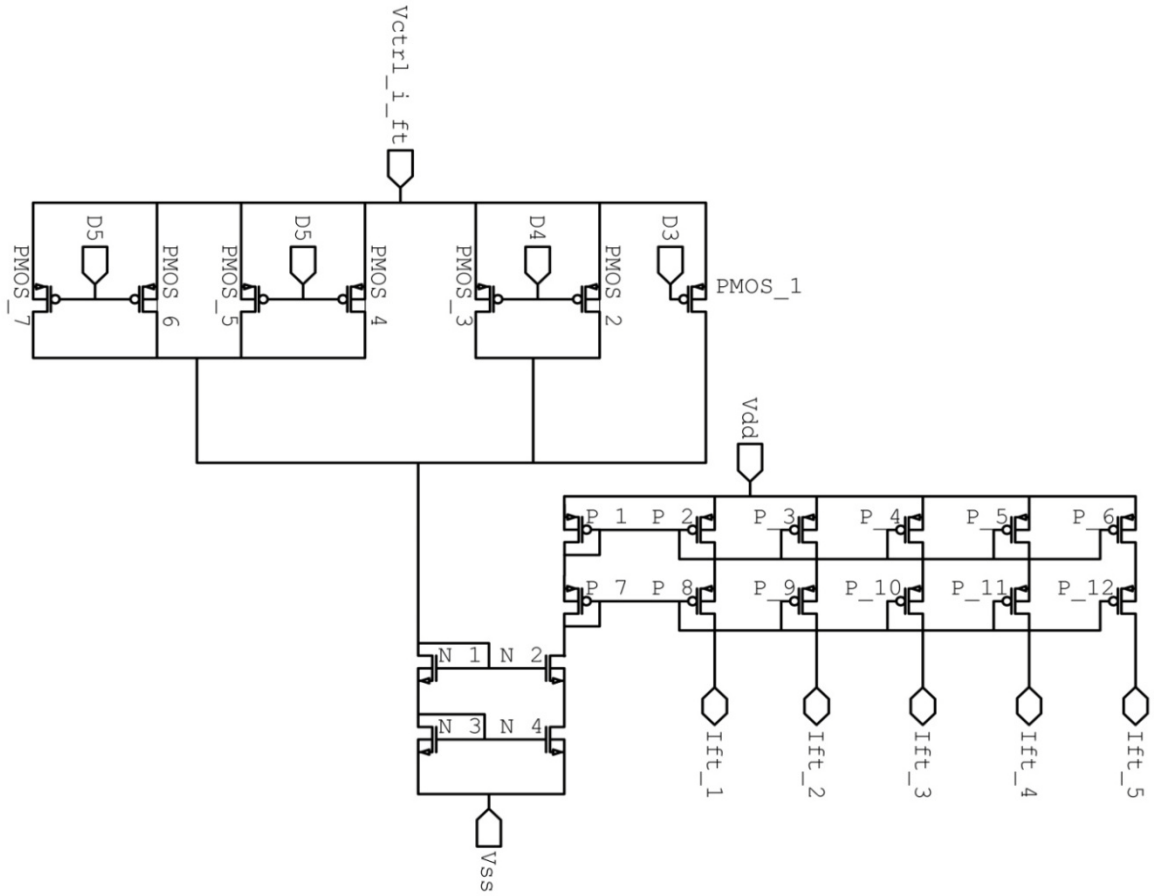


Figure 3.28 Digitally programmable fine tuning current for the integrator

The circuit in figure (3.29) is used to demonstrate multiplier/divider tunability of the bias current I_b. The circuit functions in the same way as the one used for the integrator. The three signals controlling the generated current are: $D_6, D_7\ and\ D_8$ which also depend on digital bits from the control word. The reference voltage $Vctrl\_mt$ is adjusted to a value of $268mV$ in order to mak the current generated by $PMOS\_1$, $I_6 = 0.5\mu A$. So, based on the values of $D_6 - D_8$, the tuning circuit can generate a current ranging from $0\mu A\ to\ 3.5\mu A$ in increment of $0.5\mu A$. The required two copies are generated I_{b1_t} & I_{b2_t}. The aspect ratios used are shown in table (9).

Table 9 Transistors aspect ratio of M/D tuning circuit

Transistor	W	L
$PMOS\_1\ to\ PMOS\_7$	0.5μ	20μ
$N\_1\ to\ N\_4$	10μ	0.5μ
$P\_1\ to\ P\_6$	20μ	1μ

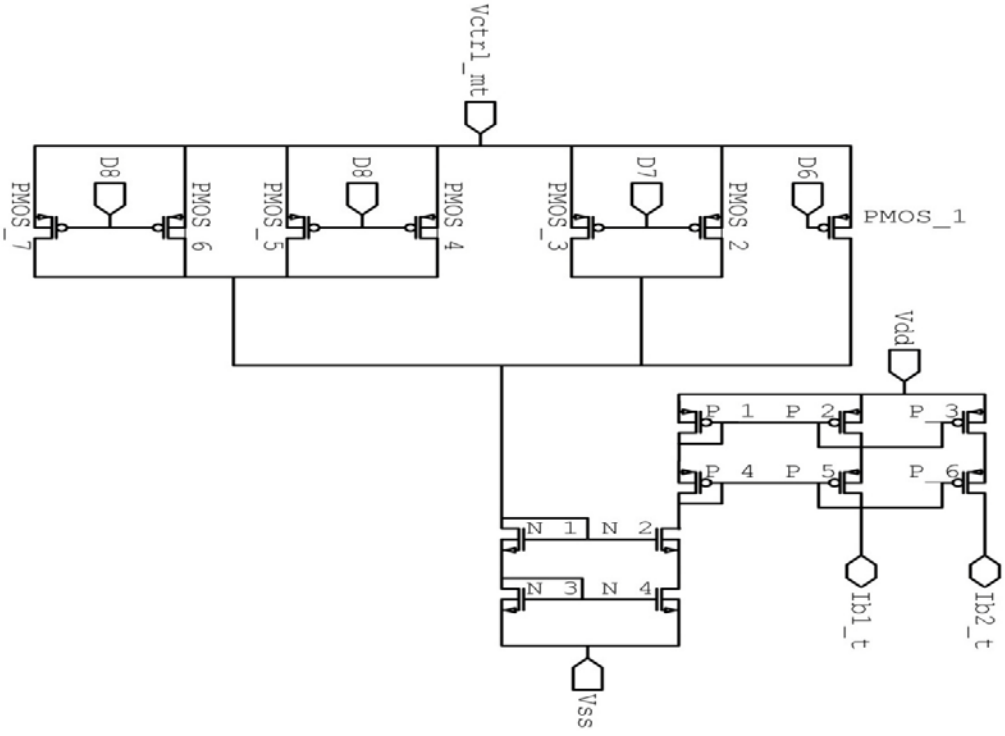


Figure 3.29 Digitally programmable current tuning for the multiplier/divider

3.3.2 Current Mirrors

The other supplementary circuits required for the sake of CAB operation are the current mirrors. Several current mirrors are built and the method used in all of them is the simple cascode mirrors. Figure (3.30) shows the current mirror circuit used to generate two equal copies of the input signal I_y. Transistors $PMOS\_1$ to $PMOS\_4$ and $NMOS\_1$ to $NMOS\_4$ create an inverted copy of I_y which is fed into the rest of the circuit to create I_y_AS *and* I_y_M directed outward. One of these two copies (I_y_AS) is used as an input to the adder-subtractor, while the other copy (I_y_M) is used as an input to the multiplier/divider. The aspect ratios of the transistors are: $^{6\mu}/_{0.5\mu}$ for all PMOS and $^{3\mu}/_{0.5\mu}$ for all NMOS.

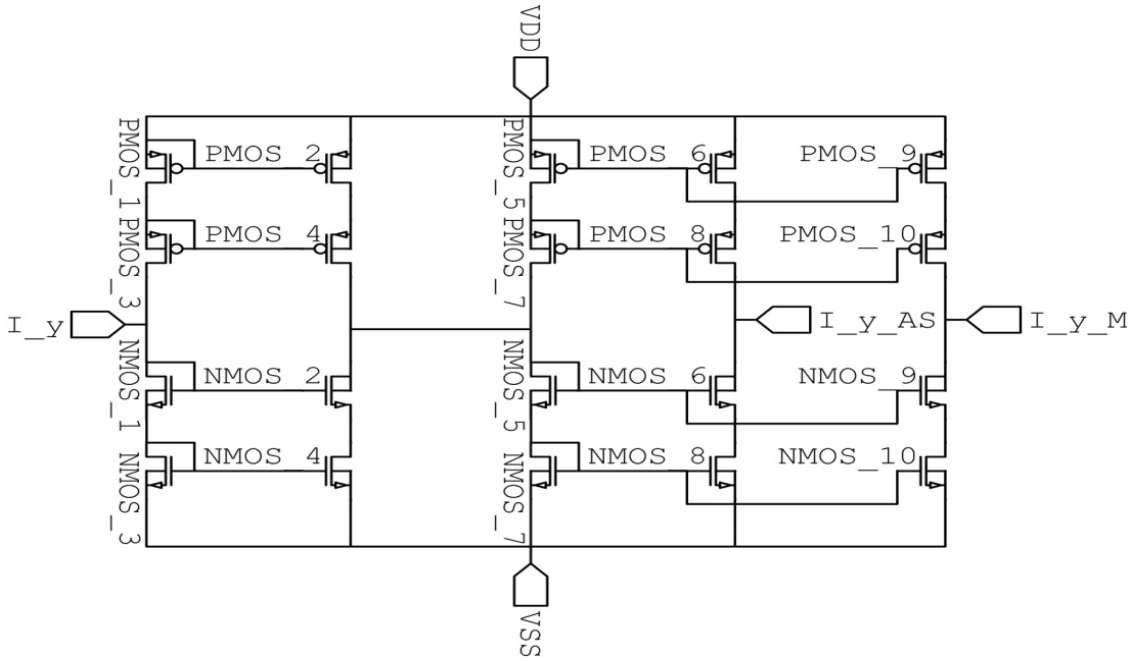


Figure 3.30 Current mirror for input current I_y

The circuit in figure (3.31) is used to produce the required four copies of the input I_x to be used in the multiplier/divider. These copies are as follows:

- $I\_2x\_1 = 2 * I_x$ $(directed\ inward)$
- $I\_2x\_2 = 2 * I_x$ $(directed\ inward)$
- $I\_x\_1 = I_x$ $(directed\ outward)$
- $I\_x\_2 = I_x$ $(directed\ outward)$

The aspect ratios of the transistors are: ${}^{6\mu}/_{0.5\mu}$ for all PMOS and ${}^{3\mu}/_{0.5\mu}$ for all NMOS. All the transistors are assigned a multiplicity of $M = 1$ except transistors $PMOS\_2, PMOS\_4, PMOS\_5, PMOS\_6$ and $NMOS\_2, NMOS\_4, NMOS\_5, NMOS\_6$ which are assigned $M = 2$ in order to get the $2 * I_x$ version.

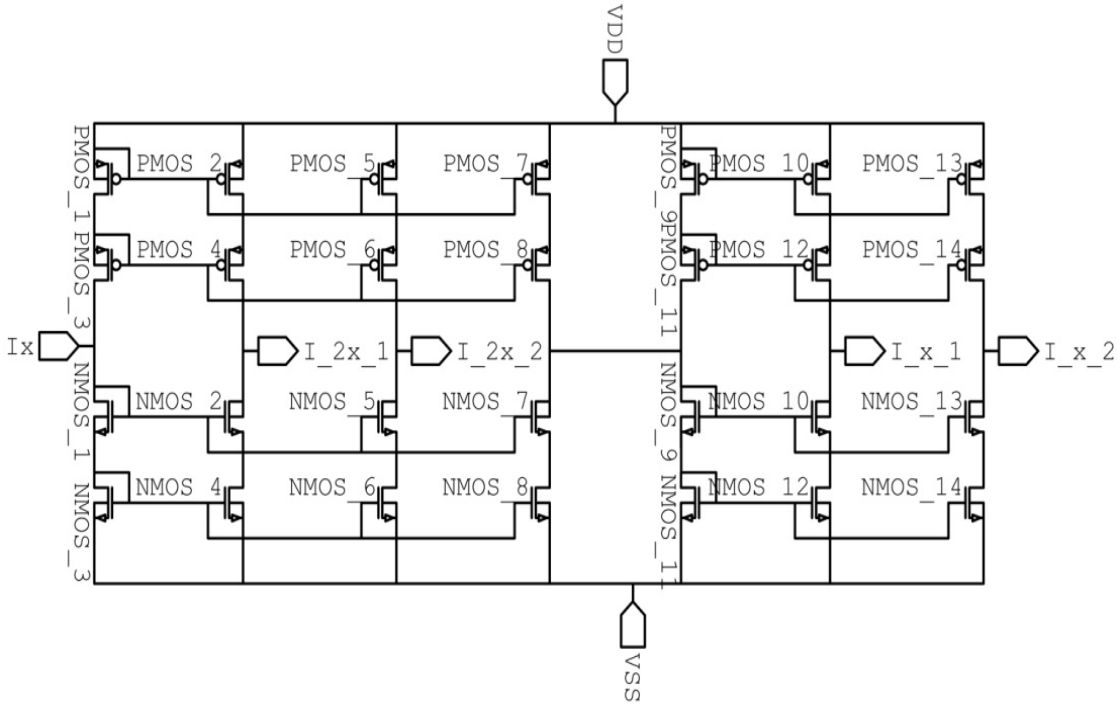


Figure 3.31 Current mirror for multiplier/divider input Ix

The mirror in figure (3.32) is the same as the circuit in figure (3.31) but with different multiplicities assigned. It is used to create the required four copies of the input I_y to be used in the multiplier/divider. These copies are as follows:

- $I\_2y\_1 = 2 * I_y$ $(directed\ inward)$
- $I\_y\_1 = I_y$ $(directed\ inward)$
- $I\_2y\_2 = 2 * I_y$ $(directed\ outward)$
- $I\_y\_2 = I_y$ $(directed\ outward)$

The aspect ratios of the transistors are: ${}^{6\mu}/_{0.5\mu}$ for all PMOS and ${}^{3\mu}/_{0.5\mu}$ for all NMOS. Transistors $PMOS_5$, $PMOS\_6$, $PMOS\_10$, $PMOS\_12$ and $NMOS\_5$, $NMOS\_6$, $NMOS\_10$, $NMOS\_12$ are assigned multiplicity of $M = 2$ inorder to get the $2 * I_y$ version while the remaining ones have $M = 1$.

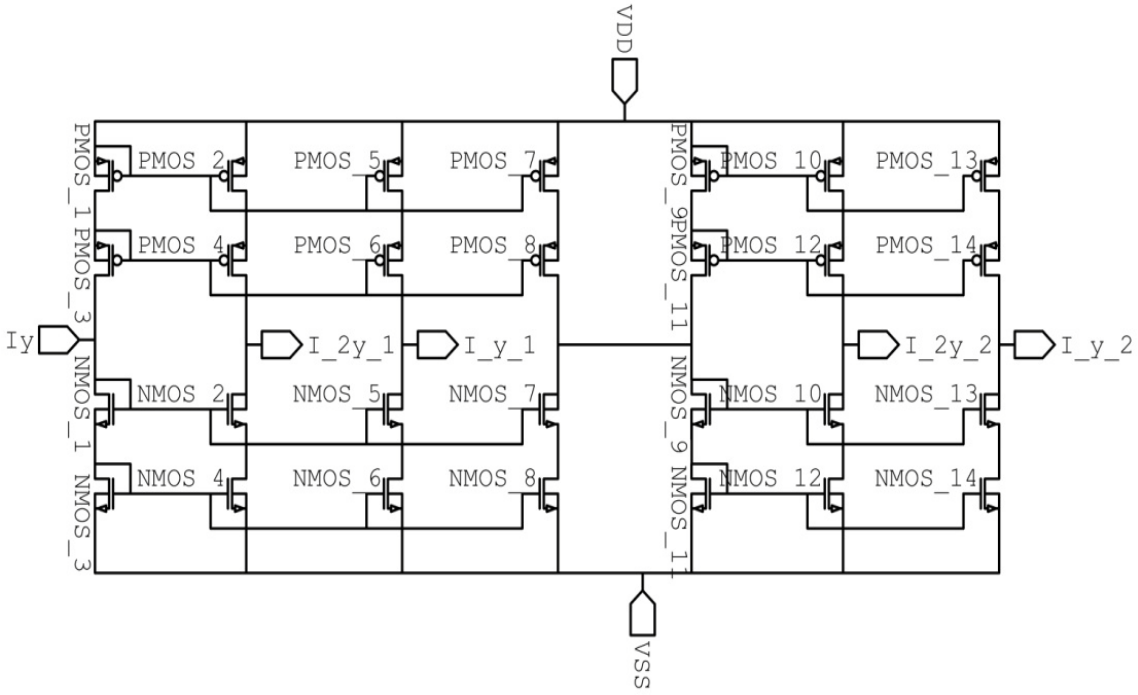


Figure 3.32 Current mirror for multiplier/divider Input Iy

In most of the applications, usually more than one copy of the output of the CAB is needed. The circuit in figure (3.33) shows the current mirrors used to create the different copies of the output of the CAB I_{out} . These copies are as follows:

- $I_{out\,1-} = I_{out}\ (directed\ inward)$
- $I_{out\,2-} = I_{out}\ (directed\ inward)$
- $I_{out\,1+} = I_{out}\,(directed\ outward)$
- $I_{out\,2+} = I_{out}\ (directed\ outward)$
- $I_{out\,3+} = I_{out}\ (directed\ outward)$

The aspect ratios of the transistors are: $^{6\mu}/_{0.5\mu}$ for all PMOS and $^{3\mu}/_{0.5\mu}$ for all NMOS. All the transistors are assigned a multiplicity of $M = 1$.

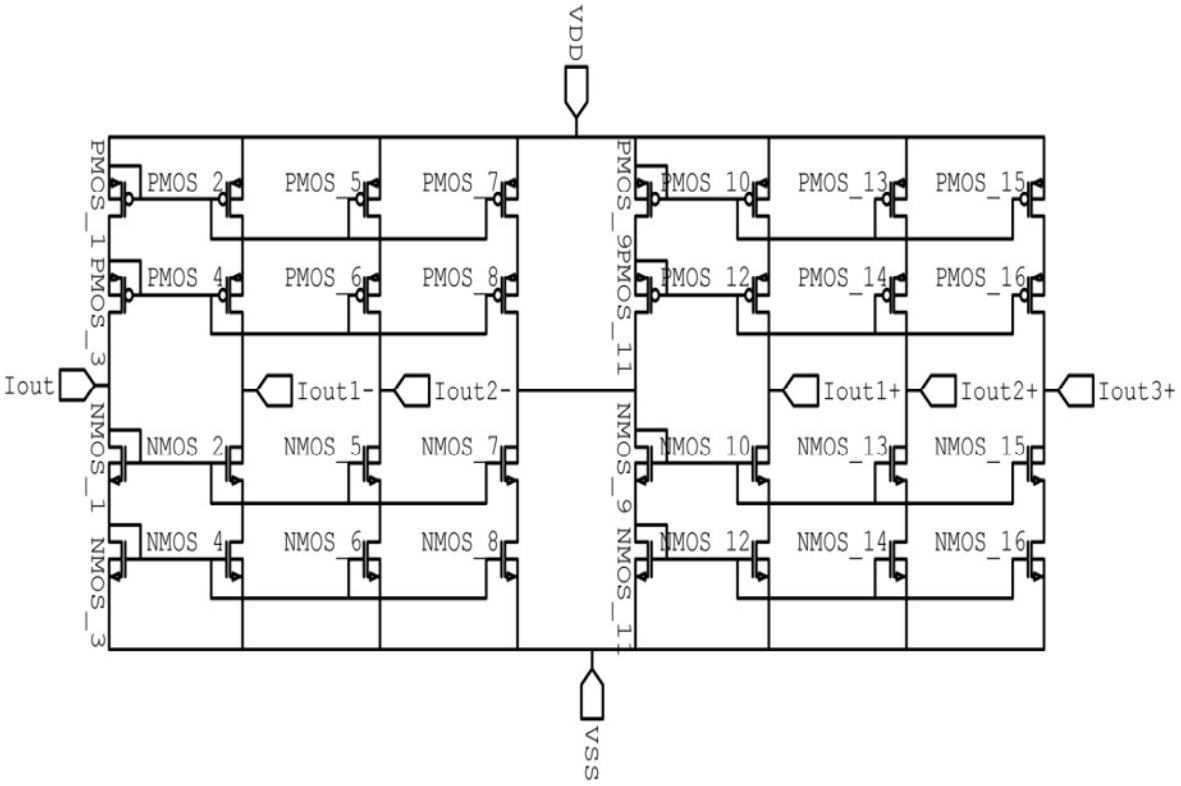


Figure 3.33 Current mirror for CAB output Iout

3.4 CAB Structure:

The CAB circuitry is structured in a unique way. It consists mainly of the three cells connected in series where each is capable of processing some function on the input signal or just passing it to the next cell. The first cell is the adder-subtractor cell in which the input will be injected first. A block diagram of this cell is shown in figure (3.34). The input I_y of this cell will be coming from current mirrors as shown in the general arrangement block diagram of figure (3.39).

When simulating the complete A/S cell with practical current sources and programming circuit built, the results reported are:

- Power consumption is 360µW, 359µW and 84µW for addition, subtraction and pass respectively.
- The worst case bandwidth is 340MHz in the case of subtraction.

From above results, it is clear that the power consumption has increased and the bandwidth has decreased compared to the performance of the circuit with ideal current sources in figure (3.1). This is due to the parasitic effect introduced by the supplementary circuits. However, the performance deterioration is not very drastic and the circuit is still at excellent level.

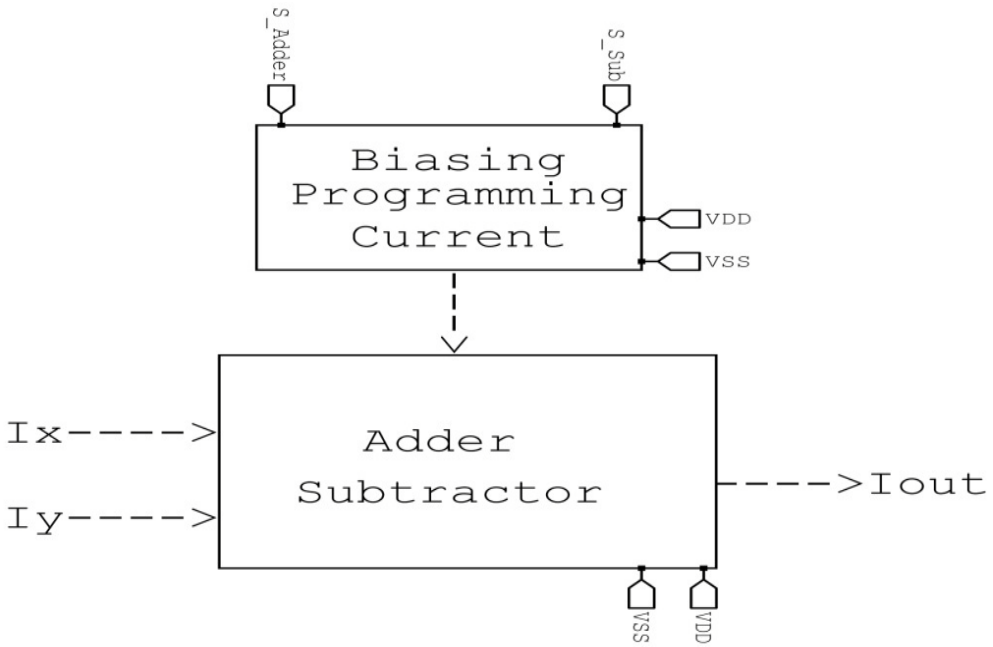


Figure 3.34 Adder-subtractor cell

The output of the A/S cell is connected to the next cell which is the integrator. The block diagram of the integrator cell is shown in figure (3.35) whose output is connected to the next cell.

When simulating the complete INT cell with practical current sources, programming circuits and tuning currents, the results reported are:

- Power consumption is 397µW
- The bandwidth is from 30 kHz to about 1GHz.

In addition, the transient simulation result is shown in figure (3.36).From the results, it is clear that the power consumption has increased and the bandwidth has decreased compared to the performance of the circuit with ideal current sources in figure (3.8).

However, the performance deterioration is not very drastic and the circuit is still at excellent level.

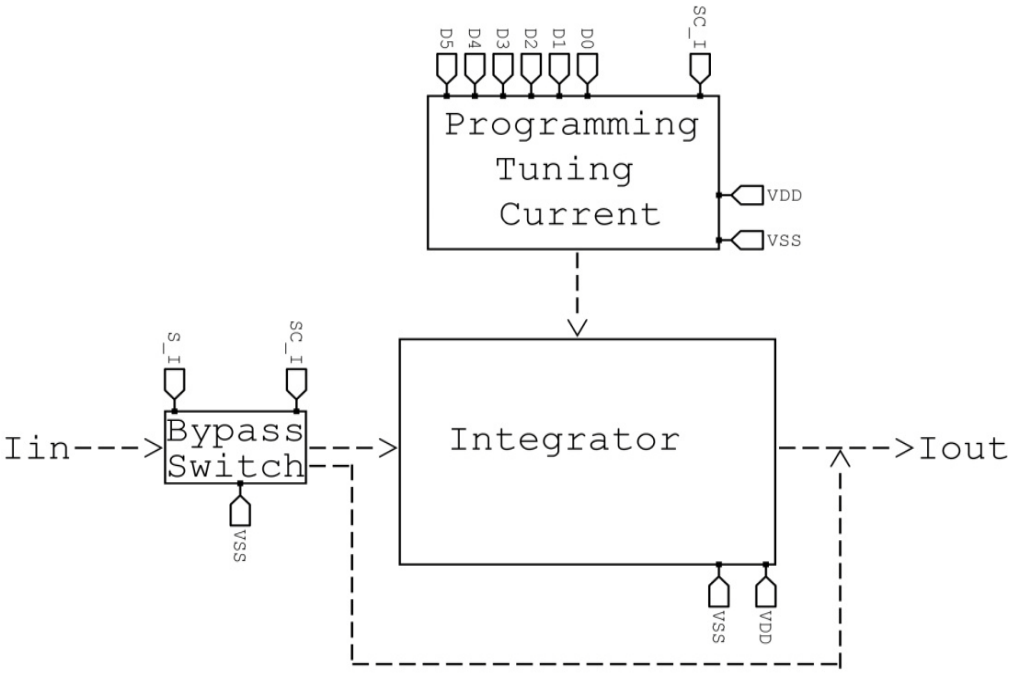


Figure 3.35 Integrator cell

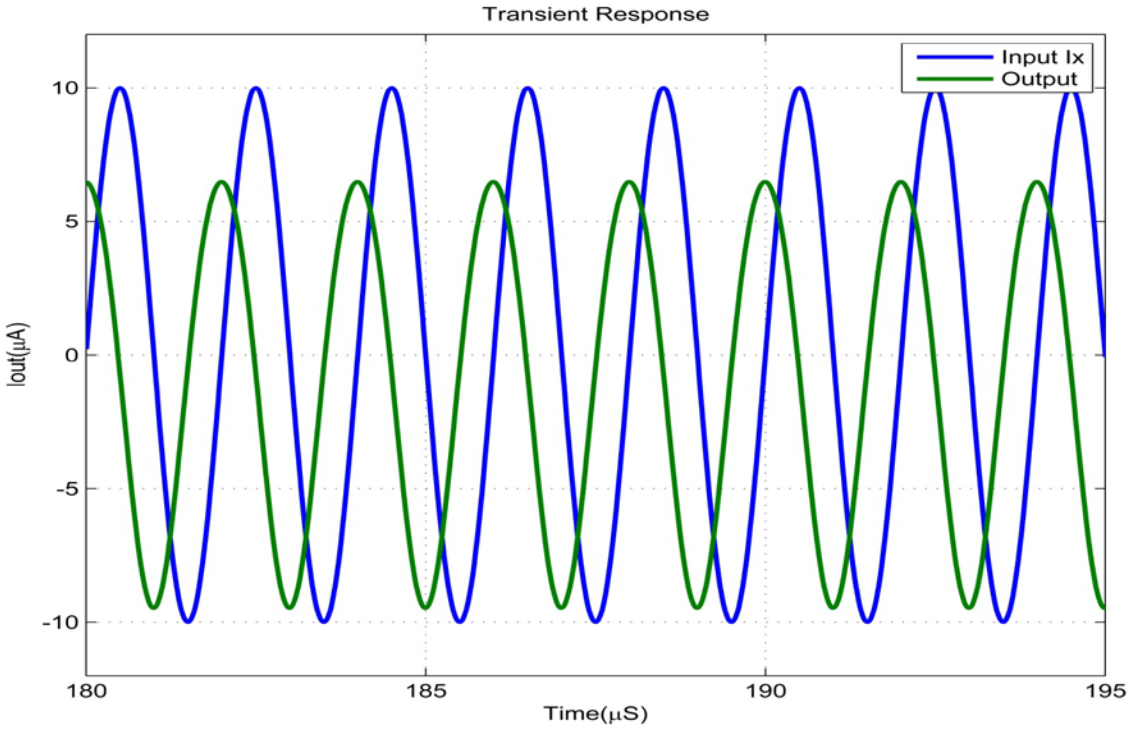


Figure 3.36 Transient response of complete integrator cell with practical sources.

The third cell block diagram is shown in figure (3.37) which represents the multiplier/divider cell. The input I_y is coming from current mirror as shown in figure (3.39). At the end the output of the multiplier/divider cell is connected to the output current mirrors as shown in the general arrangement figure (3.39).

When simulating the complete M/D cell with practical current sources, programming switches and current mirrors, the results reported are:

- Power consumption is 623µW.
- The bandwidth is 89MHz.

In addition, the DC transfer characteristic is shown in figure (3.38).From above results, it is clear that the power consumption has increased and the bandwidth has decreased compared to the performance of the circuit with ideal current sources in figure (3.13). this is due to the parasitic effect introduced by the current mirrors used. This decrease in the bandwidth in this cell is the major source of bandwidth decrease in the overall CAB. This can be solved using low parasitic structure of current mirrors which can be as future work development.

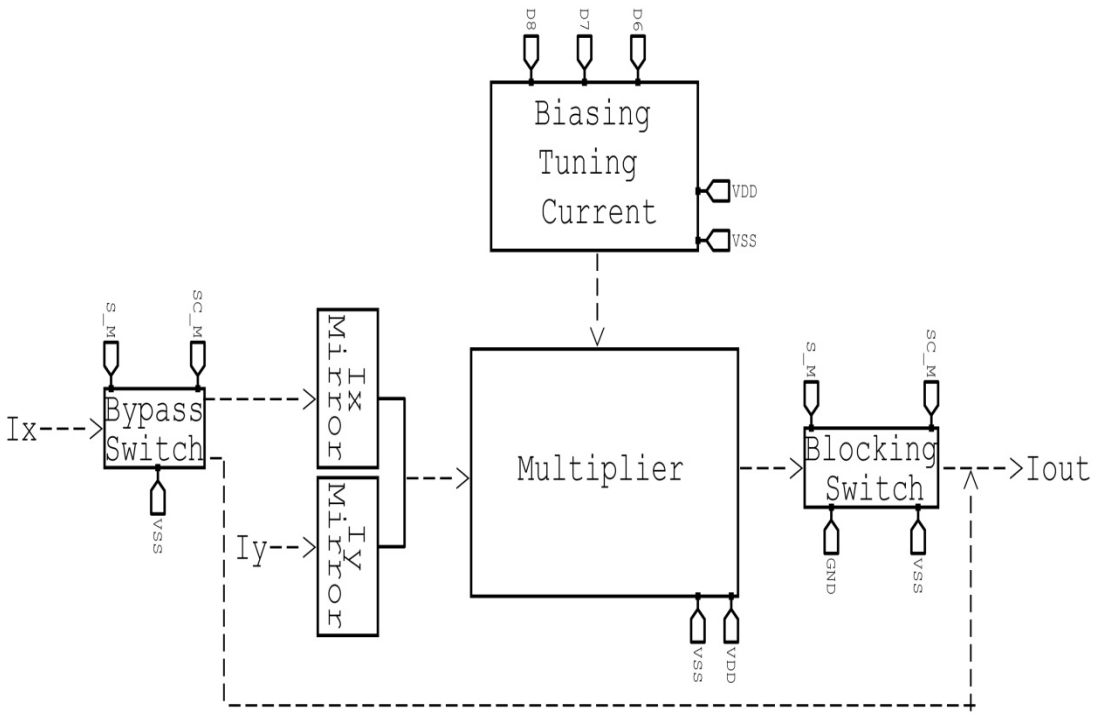


Figure 3.37 Multiplier/divider cell

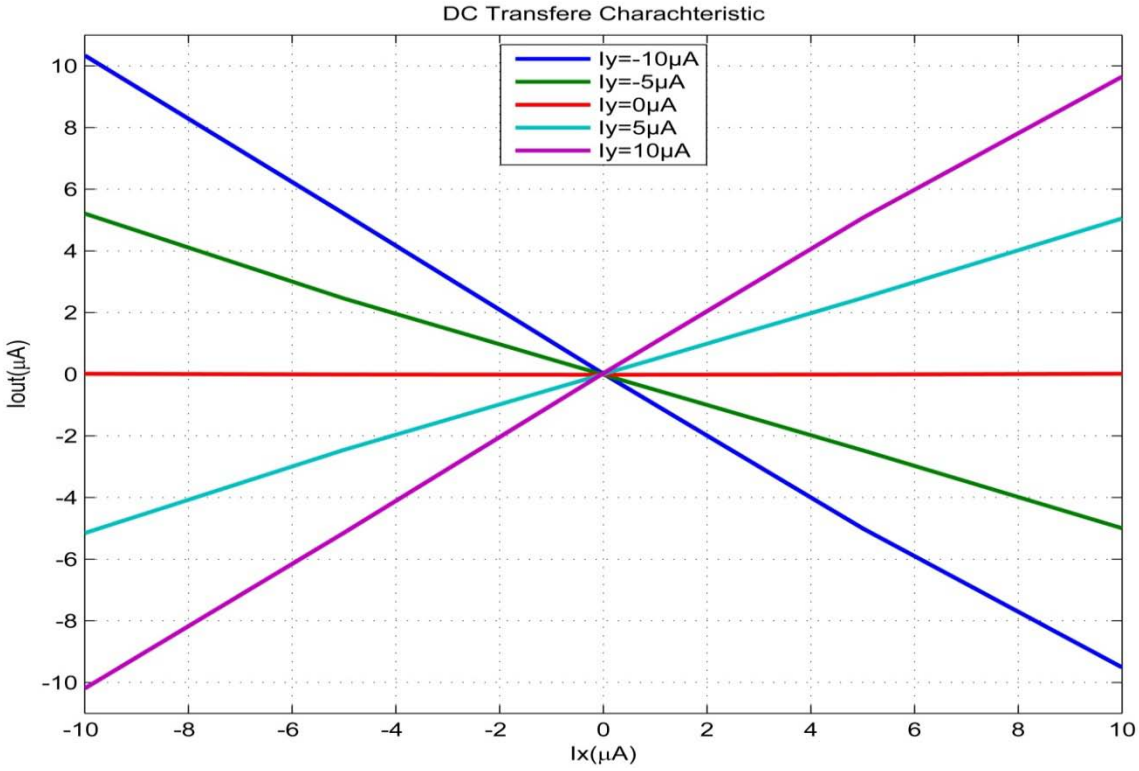


Figure 3.38 DC characteristic of complete M/D cell with practical sources

Figure (3.39) shows how all the cells are arranged to form the CAB circuitry. Using this architecture, enables the CAB to implement a single function, double functions and triple functions since the three cells are in series.

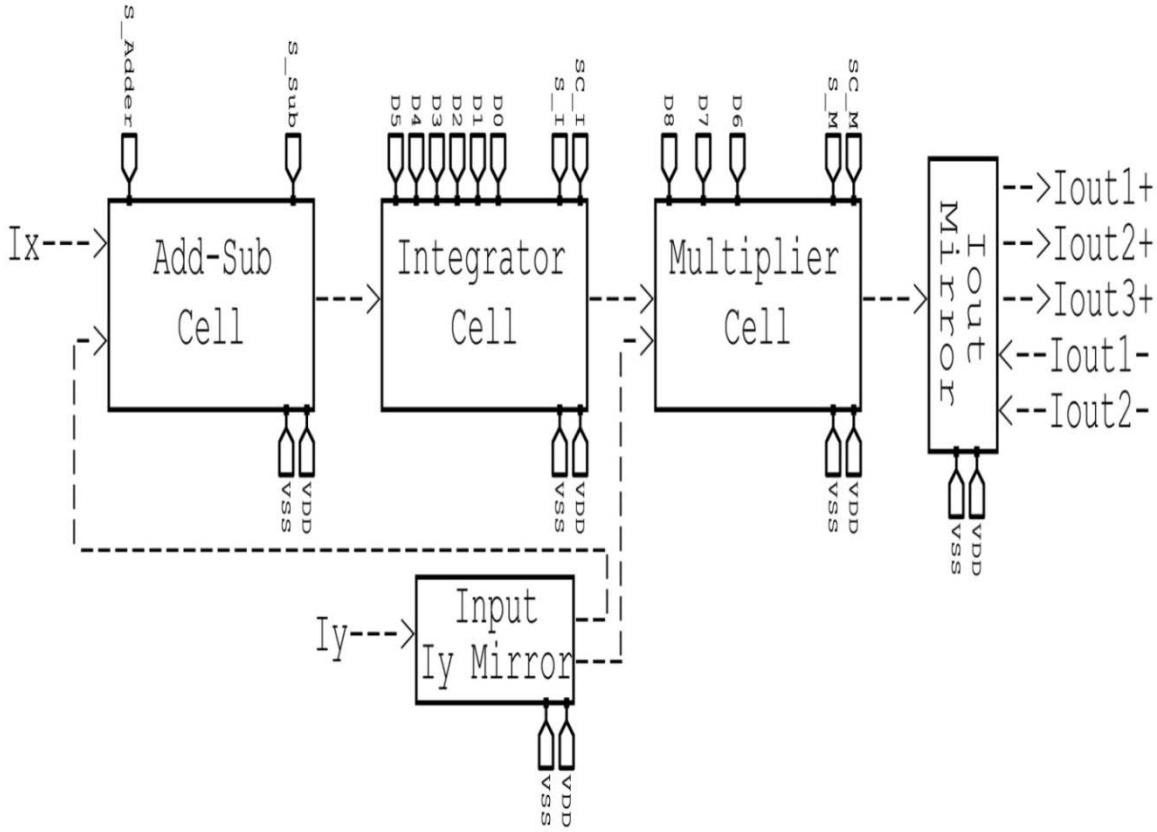


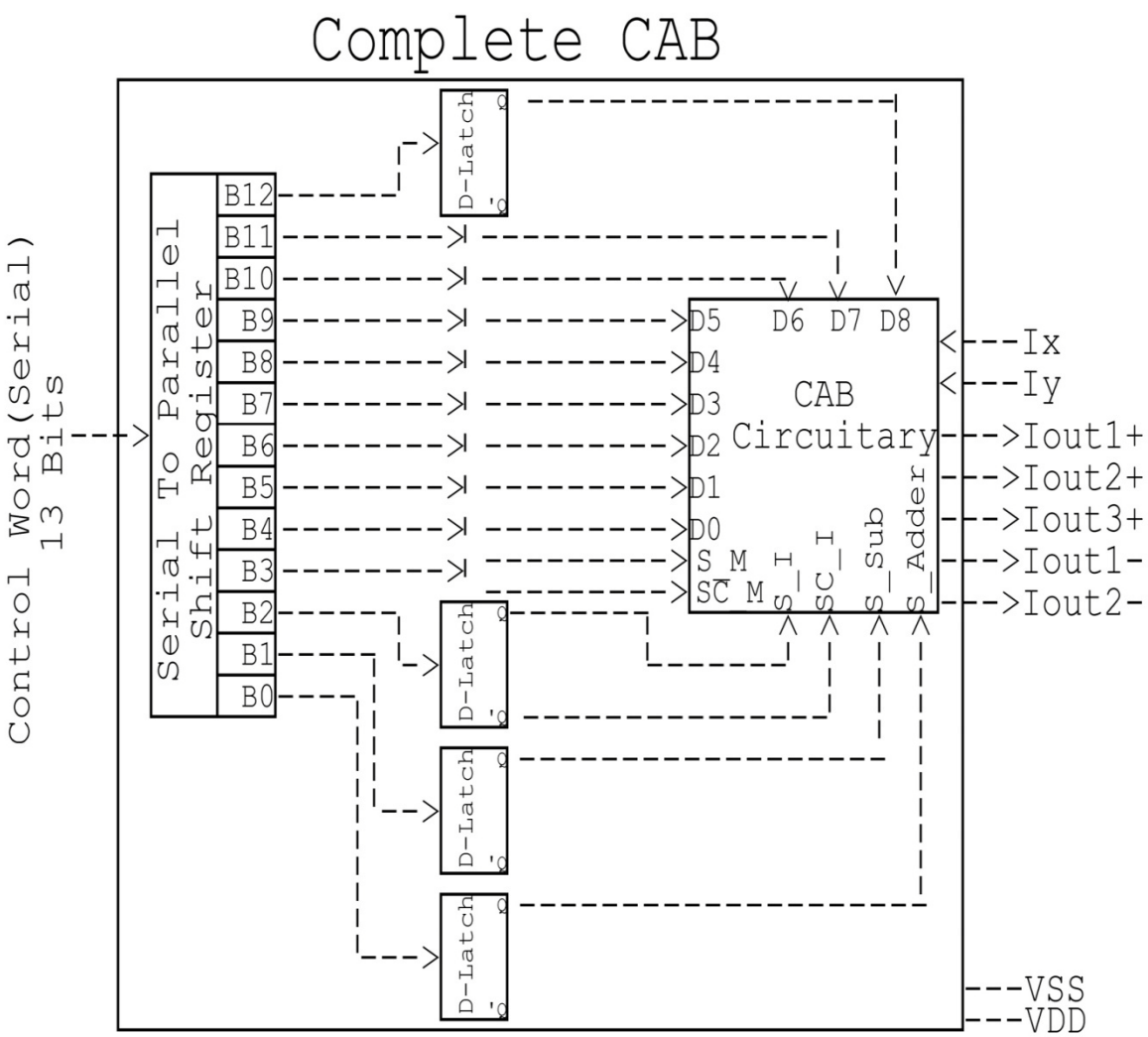
Figure 3.39 CAB general arrangement of all cells forming the CAB circuitry

The complete CAB control word consists of 13 bits. It is divided into two parts: the programming part and the tuning part. The programming part consists of four digits which are responsible for determining the mode of operation of the CAB. The tuning part consists of nine digits which are responsible for tuning the parameters of the selected function. The first six digits of the control word tuning part are devoted for the integrator biasing current (I_c) tuning, three for coars tuning and three for fine tuning. The remaing three digits of the tuning part are for multiplier/divider biasing current (I_b) tuning.

Assuming that these 13 bits are to be the input to a serial to parallel shift register, each bit at the output of the serial-In/parallel-out register is stored in a memory element (D-Latch). The outputs of the D-Latches are connected to the appropriate nodes in the CAB circuitry. Figure (3.40) presents the complete picture of the CAB starting from the control word input. The overall CAB requires 10 pins on the chip which are: $V_{dd}, V_{ss}, I_x, I_y, I_{out\,1-}, I_{out\,2-}, I_{out\,1+}, I_{out\,2+,} I_{out\,3+}$ and the control word input.

Care must be taken when using the control word since some words are not allowed. When the integrator is in its OFF state, the tuning currents should also be deactivated otherwise wrong results will be gained. As a result, the following stipulation should be taken into consideration when using the control word:

- Whenever B_2 is at logic 0, then $B_4\ up\ to\ B_9$ must be at logic 1.



Control Word

9 bits for tunability (parameters tuning)									4 bits for programmability			
3 bits for multiplier biasing current (Ib) tuning			6 bits for integrator biasing current (Ic) tuning									
			Fine tuning			Coars tuning						
D8	D7	D6	D5	D4	D3	D2	D1	D0	S_M	S_I	S_Sub	S_Adder
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Figure 3.40 Complete CAB with the control word

3.5 CAB Feature Comparison

In this chapter, the design of configurable analog block has been proposed. The CAB is based on current mode CMOS transistors operating in strong inversion. Comparison between the features of the proposed design and previously reported designs is presented in table (10).

The designs reported in [11, 26] are based on the same method adopted in the proposed design. However, the proposed CAB enjoys better features especially in terms of bandwidth and size. The design in [5] exhibits better bandwidth than the proposed CAB, however this is due to the fact that [5] adopts BJT technology rather than CMOS. Moreover, the introduced design consumes low power and it is suitable for integration since it uses only MOSFET transistors and a grounded capacitor. In addition, the proposed CAB is expected to be useful in many filter application, continuous signal processing and other area. To sum up, the main attractive features of the designed CAB are large bandwidth, low power dissipation and small area.

Table 10 CAB feature comparison

Features	Ref [8,22]	Ref [7,23]	Ref [10]	Ref [11]	Ref [26,27]	Ref[5,28,32]	Proposed
Voltage	2.5 V	$\pm$0.75 V	$\pm$0.5 V	-	-	$\pm$1.5 V	$\pm$1.5 V
Max. Power Consumption	-	0.507 mW (stand by)	2.4 mW (stand by)	-	-	-	1.4 mW (at integration) 0.911 mW (standby)
Max. 3dB Bandwidth	few MHz	11.3 MHz	11.6 MHz	Below 100kHz	10MHz	100 MHz	34.9MHz
Approx. Size ($\mathbf{mm^2}$) **	0.469	-	-	0.0338	Between 0.445 and 0.89	-	0.0537
Achieved Operations *	A, S, AM, AT, I	A, S, I, F	F	A, M, TO, CM	I, AM, AT	P, A, S, I, D, E	P, A, S, I, M
Design Method	OTA based	CFOA based	Digitally prog. CCII based	Switches & transistor primitive elements	Transistor primitive	Transistor level based design	Transistor level based design
Means of Prog. and Tune.	Prog. C's and MOS switches	Prog. R's, C's and pass switches.	Direct wiring	Pass switches and variable V. sources	Branch activation via switches	Digitally modifying circuit biasing currents	Digitally modifying circuit biasing currents and some switches.
Application Area	Filter application	Filter application	Filter application	Neural network application	Filter application	Filter application	Filters, modulation-demodulation and phase detector.
Technology	2μm CMOS	0.35µm CMOS	90 nm CMOS	1.2μm CMOS	2μm CMOS	BJT	0.35μm CMOS
Operation Region	Strong inversion	saturation	saturation	Sub-threshold	saturation	active	Strong inversion
Voltage-Current Mode	Current	Voltage	Voltage	Current and voltage	Current	Current	Current

*P=pass, A=addition, S=subtraction, I=integration, M=multiplication, TO=threshold operation, F=filtering, CM=coefficient multiplication, AM=amplification, AT=attenuation, D=differentiation, E=exponential,

** The proposed CAB size is approximated by 30 times the total size of transistors.

CHAPTER 4

PROPOSED APPLICATIONS

Based on the CAB designed in chapter 3, several applications are realized. These applications are meant to prove the functionality, programmability and tunability of the proposed CAB. More than one copy of the proposed CAB unit is used in each application. Each unit is configured to perform a specific operation via the control word. The combination of all the units in one application leads to the resultant required output. The presented applications are as follows:

- Universal second order Filter
- Fourth Order Band Pass Filter BPF
- Modulation and Demodulation System
- Phase Detector

All the simulation results are obtained using Tanner EDA Tools v13.0 with level 49 model parameters (BSIM3) in $0.35\mu m$ standard CMOS technology.

4.1 Universal Second Order Filter:

In this application, four CAB units are utilized to realize a second order universal filter. Figure (4.1) shows how these CABs are connected to each other in which no other components apart from the CABs are required. The realized universal filter is capable of performing low pass (LPF), high pass (HPF), band pass (BPF), band reject and all pass filter (APF).

In the referred figure, CAB_1 is configured as a pass cell while $CAB_2 and\ CAB_3$ are both configured as integrators. Only using these three CABs, LPF, HPF and BPF can be obtained. By Using CAB_4 and configuring it to work as a subtractor, we can obtain the remaining two filter types which are band reject and APF. This arrangement to realize a universal filter is reported with slight modifications in many publications [32, 43 and 60].

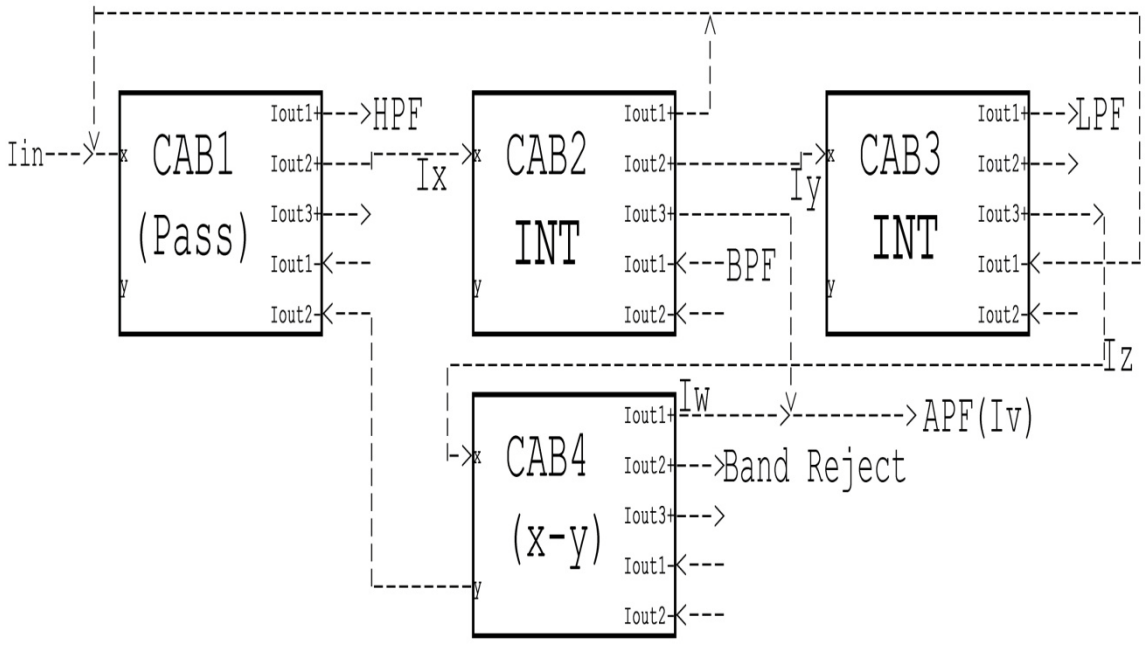


Figure 4.1 Universal second order filter block diagram

From figure (4.1):

$$I_y = -I_x * \frac{A}{S} \tag{4.1}$$

$$I_z = -I_y * \frac{A}{S} \tag{4.2}$$

$$I_x = I_{in} + I_y - I_z \tag{4.3}$$

Substituting equation (4.1) and (4.2) into (4.3) results in:

$$I_{in} = I_x - \left(-I_x * \frac{A}{S}\right) + (-I_y * \frac{A}{S}) \tag{4.4}$$

$$I_{in} = I_x + \left(I_x * \frac{A}{S}\right) + (I_x * \frac{A}{S} * \frac{A}{S}) \tag{4.5}$$

$$I_{in} = I_x(1 + \frac{A}{S} + \frac{A^2}{S^2}) \tag{4.6}$$

$$\frac{I_x}{I_{in}} = \frac{S^2}{S^2+AS+A^2} \tag{4.7}$$

Equation (4.7) clearly represents the transfer function of a HPF. Now using I_x from equation (4.1) into equation (4.7):

$$\frac{I_y}{I_{in}} = \frac{-AS}{S^2+AS+A^2} \tag{4.8}$$

Therefore, equation (4.8) represents a BPF. In addition, using port ($I_{out\,1-}$) of CAB_2 which gives $(-I_y)$ we can get a non inverting transfere function as follows:

$$\frac{-I_y}{I_{in}} = \frac{AS}{S^2+AS+A^2} \tag{4.9}$$

Now using I_y from equation (4.2) into equation (4.8):

$$\frac{I_z}{I_{in}} = \frac{A^2}{S^2+AS+A^2} \tag{4.10}$$

Equation (4.10) models a LPF.

$$I_w = I_z - (-I_x) \tag{4.11}$$

Therefore,

$$\frac{I_w}{I_{in}} = \frac{I_z+I_x}{I_{in}} = \frac{S^2+A^2}{S^2+AS+A^2} \tag{4.12}$$

This is the transfer function of a band reject (notch) filter.

$$I_v = I_w + I_y \tag{4.13}$$

$$\frac{I_v}{I_{in}} = \frac{I_w+I_y}{I_{in}} = \frac{S^2-AS+A^2}{S^2+AS+A^2} \tag{4.14}$$

Equation (4.14) models an APF.

The five filtering functions HPF, BPF, LPF, band reject and APF are represented with the currents $I_x, I_y, I_z, I_w \; and \; I_v$ respectively.

From the characteristic equation of all filters, the quality factor Q=1 and the center frequency $w_o = A$. The integrator unity gain frequency (A) depends on the capacitor used in the integrator and its trans-conductance g_m which is tunable by the biasing current I_c as explained in the integrator design in chapter 3.

Figure (4.2) shows the simulation results of the gain frequency characteristic for all filter types. All filters are simulated at center frequency of $f_o \approx 400\,kHz$ and quality factor $Q = 1$. The parameters of the first and second integrator $(CAB_2 and\ CAB_3)$ are identical $(c = 100pF\ and\ I_c = 20\mu A)$. The total power consumption of the universal filter is found to be $5.49mW$ when outputting all filter types simultaneously.

Figure (4.3) shows the simulated LPF response using various values of the integrator biasing current I_c. This bias current is adjusted using the control bits $(B_4\ to\ B_9)$ of the control word. It is therefore confirmed, that by adjusting the bias current an automatic frequency control can be easily implemented. Figures (4.4 and 4.5) show this frequency tuning but for the BPF and Notch filter responses. One drawback of this filter is that its quality factor (Q) is not adjustable. This is due to the fact that Q depends on the capacitor values of the integrators which are fixed internal components.

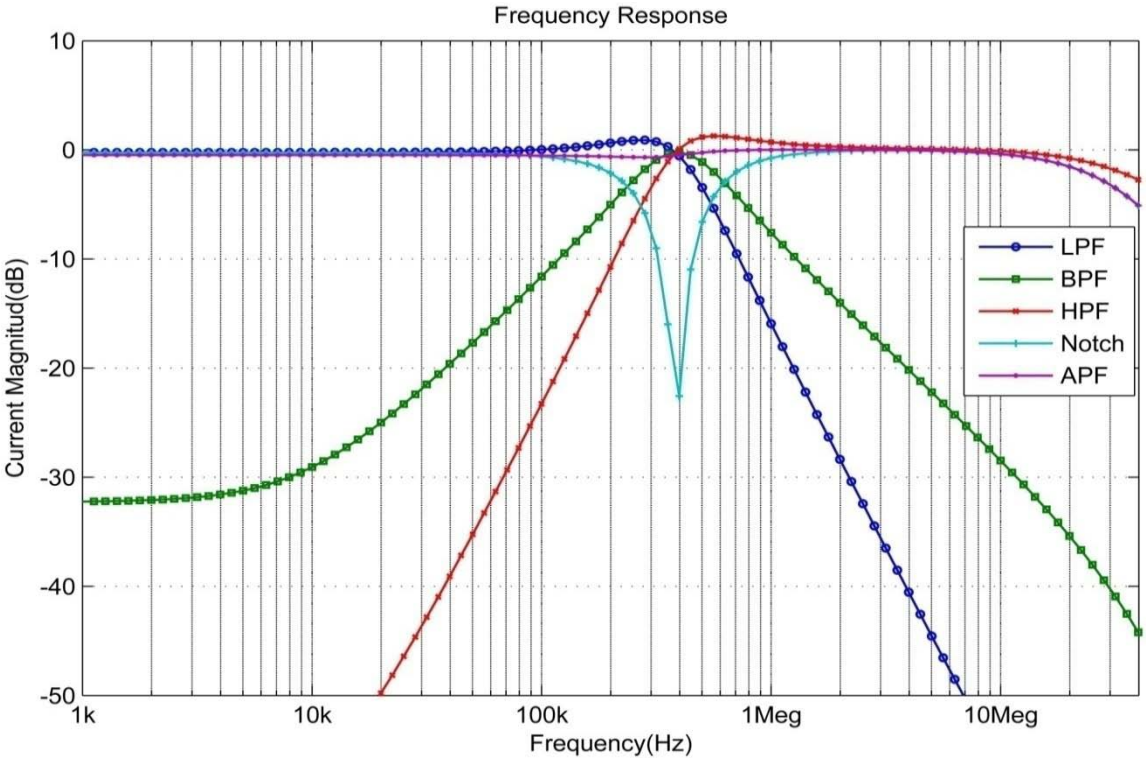


Figure 4.2 Gain Frequency response of the universal filter showing all filter types

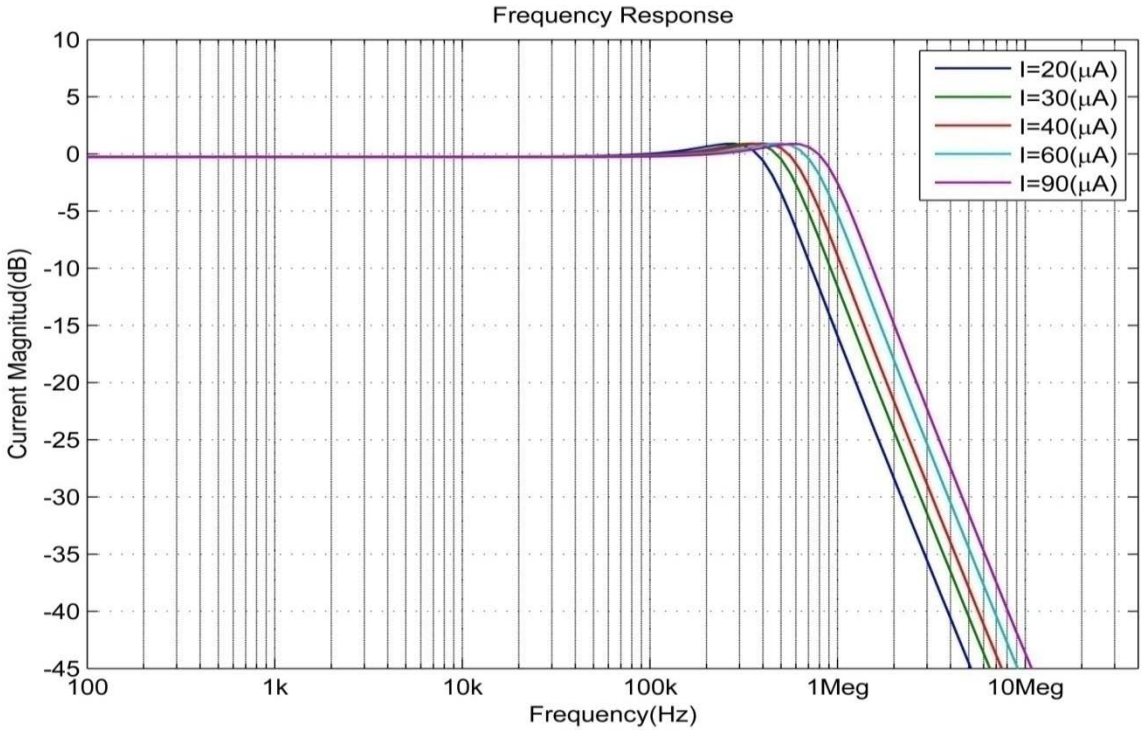


Figure 4.3 Frequency response of LPF with frequency tuning by varying Ic

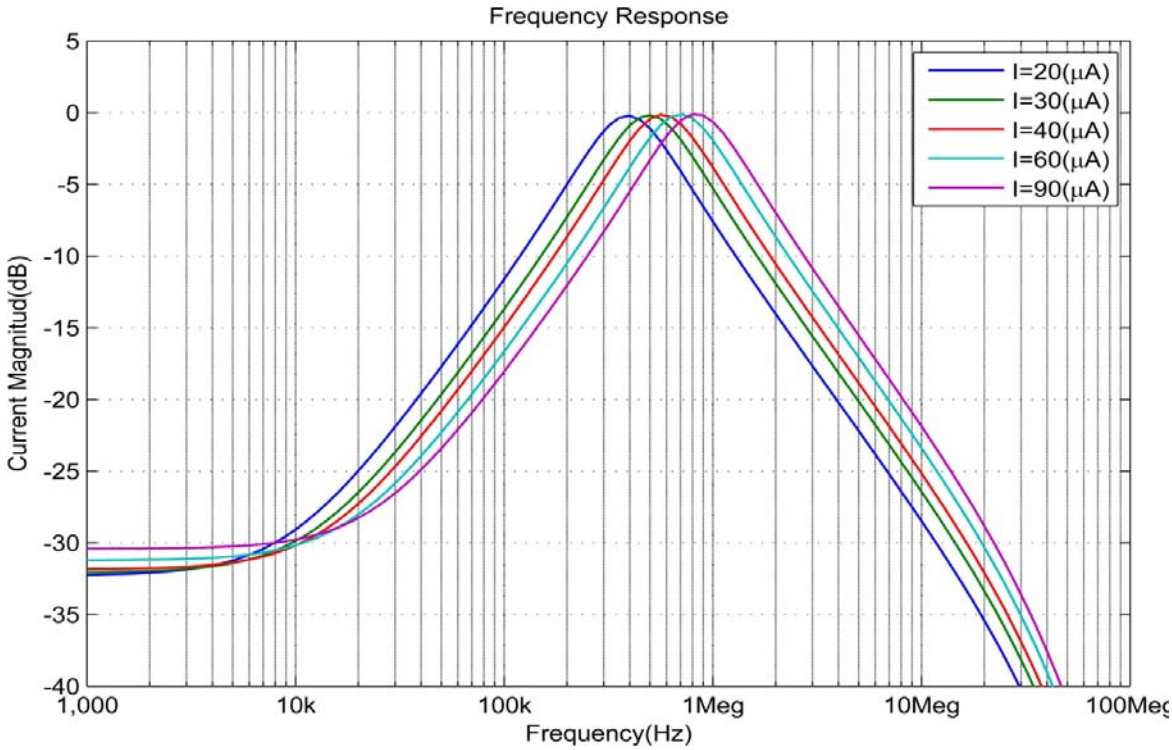


Figure 4.4 Frequency response of BPF with frequency tuning by varying Ic

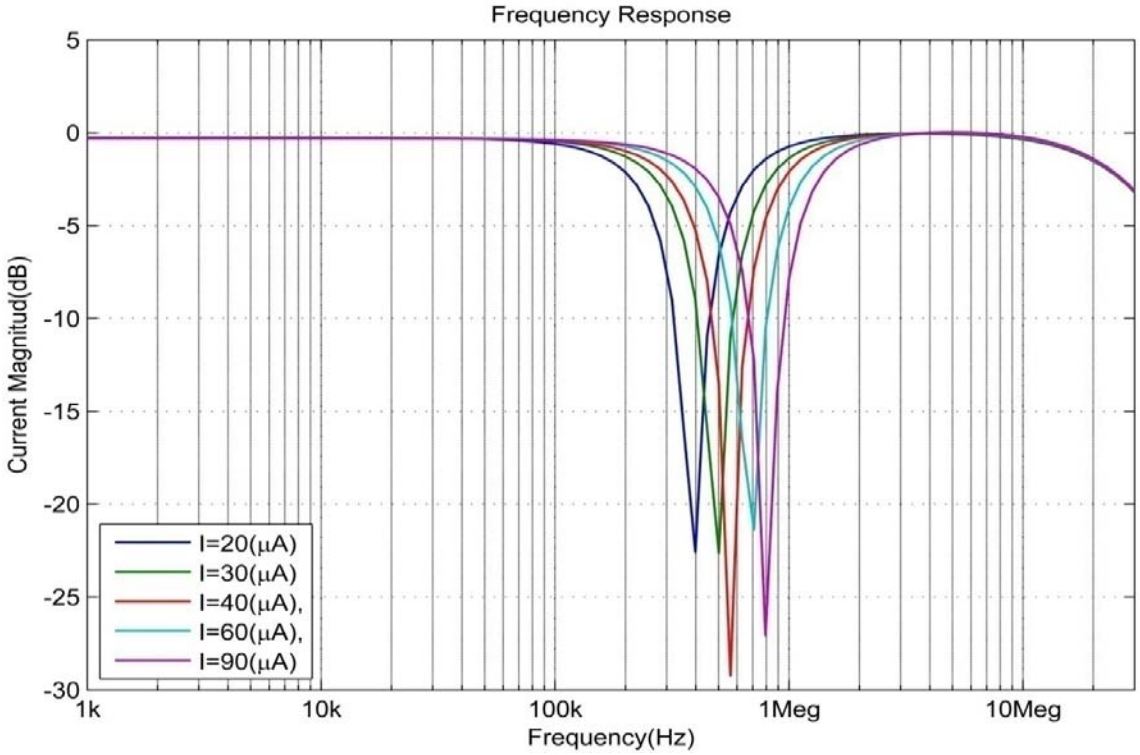


Figure 4.5 Frequency response of band reject filter with frequency tuning by varying Ic

4.2 Fourth Order Band Pass Filter:

In this application, four CAB units are utilized as integrators to realize a fourth order BPF function. Figure (4.6) shows how these CABs are connected to each other to form the filter. The realized filter is tunable in frequency via the adjustment of the bias current I_c which is done through the control word.

In the referred figure, the four integrators are cascaded and negative feedbacks are taken to the input node. The output from CAB_2 should function as a fourth order BPF.

From figure (4.6):

$$I_y = -I_x * \frac{A}{S} \tag{4.15}$$

$$I_z = -I_y * \frac{A}{S} \tag{4.16}$$

$$I_w = -I_z * \frac{A}{S} \tag{4.17}$$

$$I_v = -I_w * \frac{A}{S} \tag{4.18}$$

$$I_x = I_{in} + I_y + I_w - I_z - I_v \tag{4.19}$$

Substituting equation (4.15), (4.16), (4.17) and (4.18) into equation (4.19), results in:

$$I_{in} = \left(I_z * \frac{S^2}{A^2}\right) - \left(-I_z * \frac{S}{A}\right) - \left(-I_z * \frac{A}{S}\right) + I_z + (I_z * \frac{A^2}{S^2}) \tag{4.20}$$

$$I_{in} = I_z(\frac{S^2}{A^2} + \frac{S}{A} + \frac{A}{S} + 1 + \frac{A^2}{S^2}) \tag{4.21}$$

$$\frac{I_z}{I_{in}} = \frac{S^2A^2}{S^4+AS^3+A^2S^2+A^3S+A^4} \tag{4.22}$$

Equation (4.22) clearly represents the transfer function of a fourth order BPF. From the characteristic equation, the center frequency is $w_o = \sqrt[4]{A^4} = A$, which is tunable by the biasing current I_c.

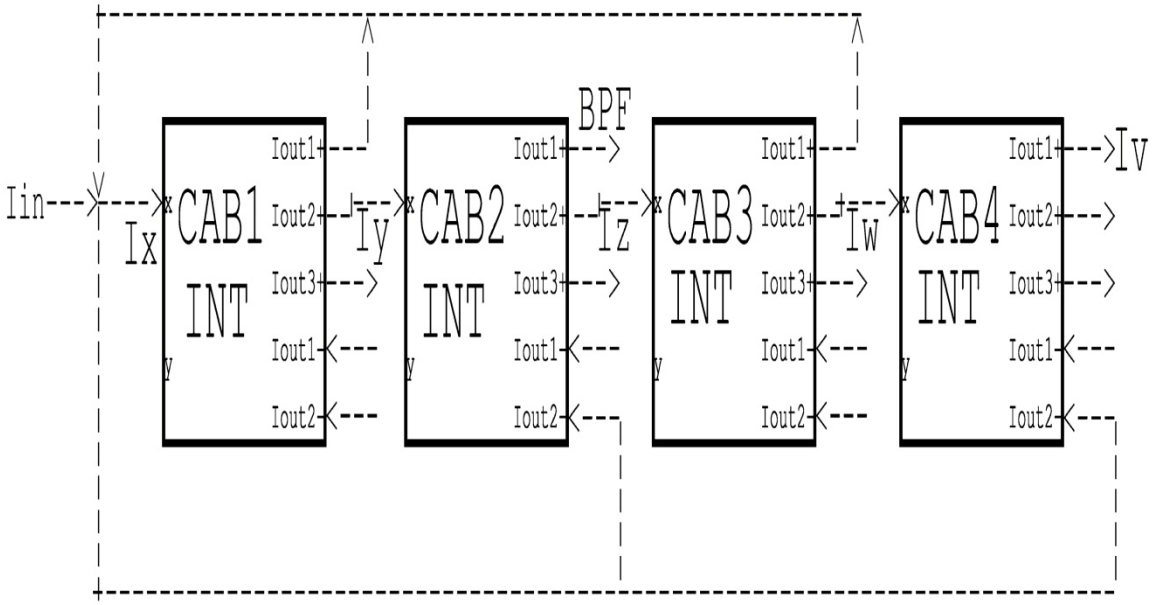


Figure 4.6 Fourth order BPF block diagram

Figure (4.7) shows the simulation results of the frequency response for the proposed BPF. It is simulated at various values of the bias current I_c which contrls the filter centr frequency. It can be seen from the graph that the slop of the filter is $\pm 40 dB/decade$ which models the characteristic for the fourth order BPF. The total power consumption of the filter when operated at the different currents with the respective center frequencies are summarized in table (11).

Table 11 Summary of resulting center frequencies and power consumption for different Ic values for the 4th order BPF

Bias current (I_c)	Power Consumption	Center Frequency(f_o)
$20\mu A$	$6mW$	$390kHz$
$30\mu A$	$6.8mW$	$490kHz$
$40\mu A$	$7.6mW$	$570kHz$
$60\mu A$	$9.3mW$	$700kHz$
$90\mu A$	$11.7mW$	$804kHz$

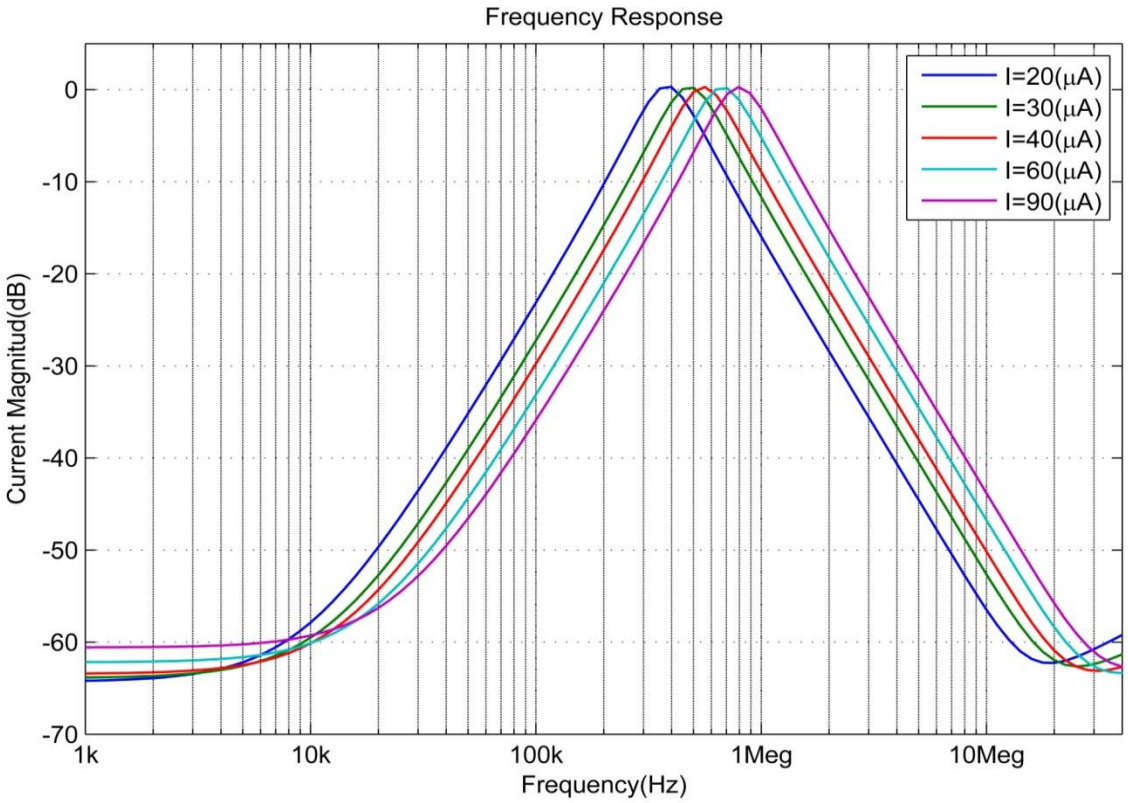


Figure 4.7 Frequency response of 4th order BPF with frequency tuning via Ic

4.3 Modulation/Demodulation System

In this application, a modulation/demodulation system is realized using the proposed CAB. Figure (4.8) shows the block diagram of the proposed system. It consists of four CAB units. CAB_1 and CAB_2 function as modulator-demodulator respectively and they are programmed to work as multipliers. The LPF is composed of CAB_3 and CAB_4 where they are configured as integrators. The connection of the LPF is presented in figure (4.9). The derivation of the LPF transfer function is the same as the previously presented in the universal filter application.

In figure (4.8), $m(t)$ is the modulating signal (the message) which is a sinusoidal with amplitude M and frequencyω_m. The carrier is $c(t)$ which is a sinusoidal signal with amplitude C and frequency ω_c. The first CAB does the modulation process and produces the modulated signal (z) as follows:

$$z = \frac{m(t)*c(t)}{I_b} = \frac{(M*C)}{2*I_b}[\sin(\omega_c + \omega_m) + \sin(\omega_c - \omega_m)] \tag{4.23}$$

The second CAB does the demodulation process to produce high frequency signals and low frequency signals as follows:

$$\frac{z*c(t)}{I_b} = \frac{c(t)}{I_b} * [\frac{M*C}{2*I_b}(\sin(\omega_c + \omega_m) + \sin(\omega_c - \omega_m))] \tag{4.24}$$

$$\frac{c(t)}{I_b} * [\frac{M*C}{2*I_b}(\sin(\omega_c + \omega_m) + \sin(\omega_c - \omega_m))] = \frac{M*C^2}{4*{I_b}^2}[\sin(2\omega_c + \omega_m) + \sin(2\omega_c - \omega_m) + 2\sin(\omega_m)] \tag{4.25}$$

It is clear from equation (4.25) that the first and second terms are the high frequency signals while the third term is the low frequency signal. In order to retrieve the message, the output of the demodulator is input to a LPF with cut off frequency higher than ω_m in order to reject the high frequency component and leave the low frequency compoenet. So, the output of the LPF is:

$$w = \frac{M*C^2}{2*I_b{}^2}\sin(\omega_m) \tag{4.26}$$

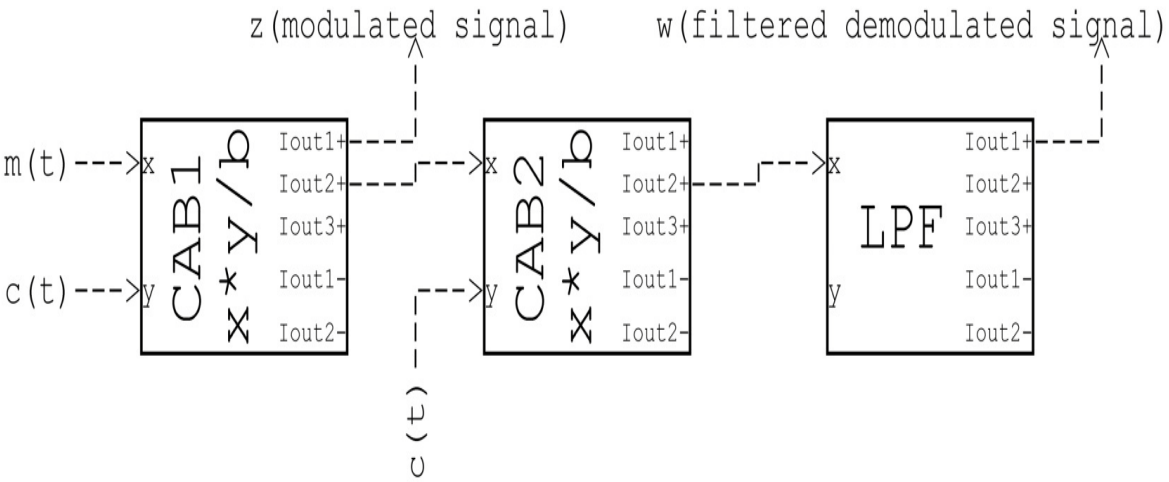


Figure 4.8 Modulation-Demodulation system block diagram

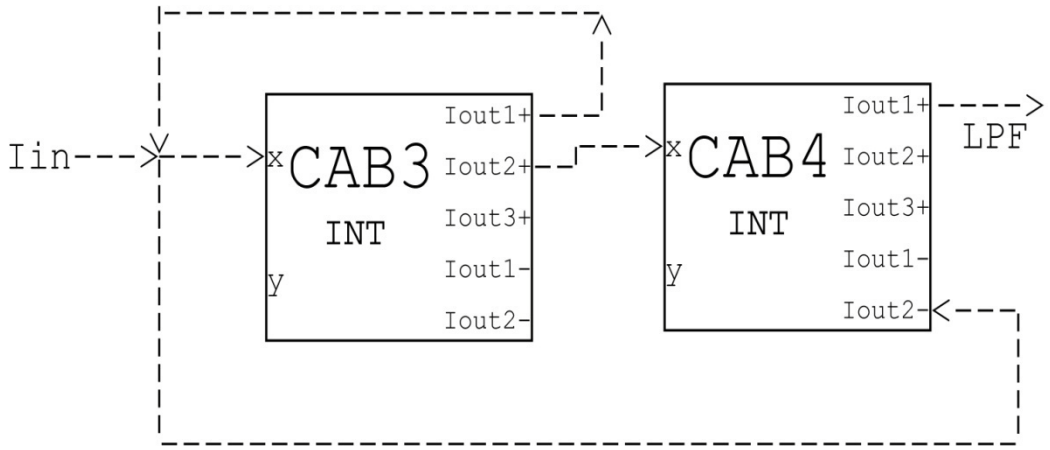


Figure 4.9 The LPF structure used in the modulation-demodulation system

In order to test the proposed system, the following parameter values are chosen: modulating signal amplitude $M = 8\mu A$ and frequency $f_m = 10kHz$, the carrier amplitude $C = 8\mu A$ and frequency $f_c = 2MHz$ and the multiplier bias current $I_b = 10\mu A$.

Figure (4.10) shows the modulating signal $m(t)$ as well as the carrier signal $c(t)$. Figures (4.11 and 4.12) show the waveform of the modulated signal (z) which is the output of CAB_1 as well as its frequency spectrum respectively. It is clear that the two main frequency components are located at $1.99MHz\ and\ 2.01MHz$ which coincide with $f_c - f_m\ and\ f_c + f_m$ respectively as per equation (4.23). The frequency spectrum of the demodulator output before applying the LPF which is taken from the output of CAB_2 is shown in Figure (4.13). The main frequency components presented in the figure are: $10kHz, 3.99MHz\ and\ 4.01MHz$ which correspond to $f_m, 2f_c - f_m\ and\ 2f_c + f_m$ respectively as per equation (4.25). The reconstructed output signal of the LPF (w) is presented in figures (4.14 and 4.15) as waveform and as frequency spectrum respectively. The specification of the low pass filter used here is the same as the one presented in the universal filter application. The total power consumption of the four CABs when realizing this application is about $5.2\ mW$.

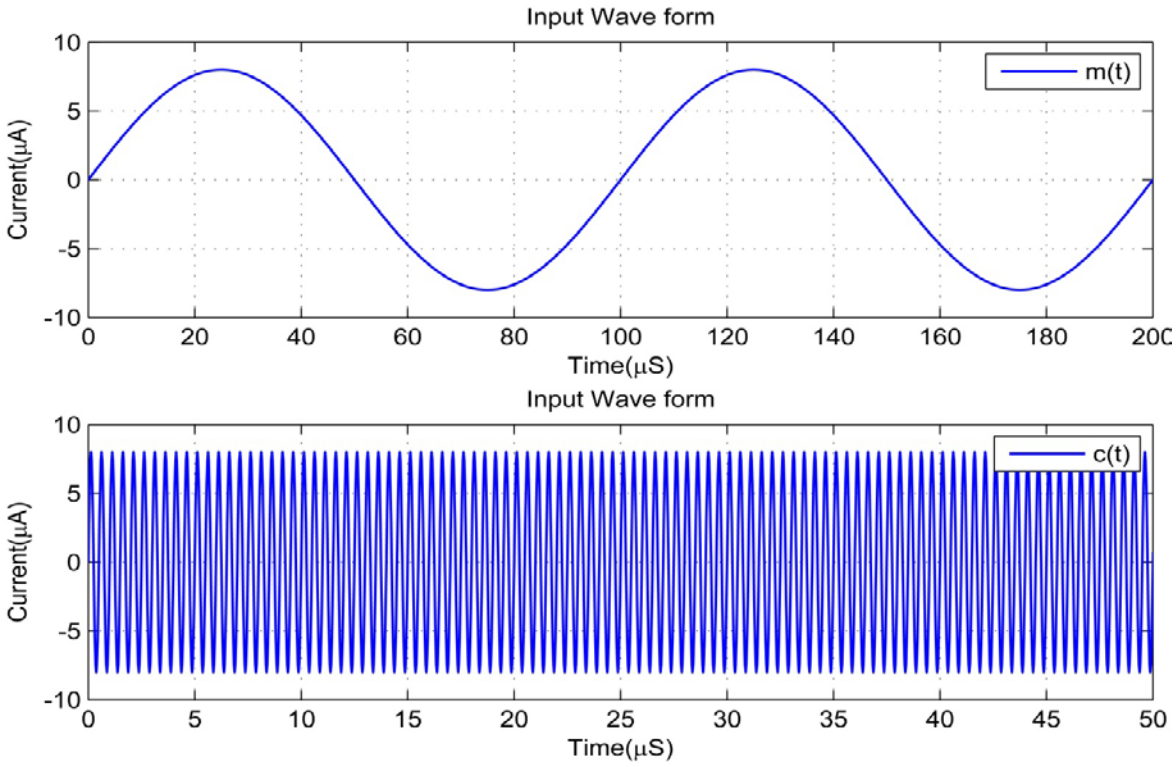


Figure 4.10 Waveforms of the modulating signal m(t) and carrier c(t)

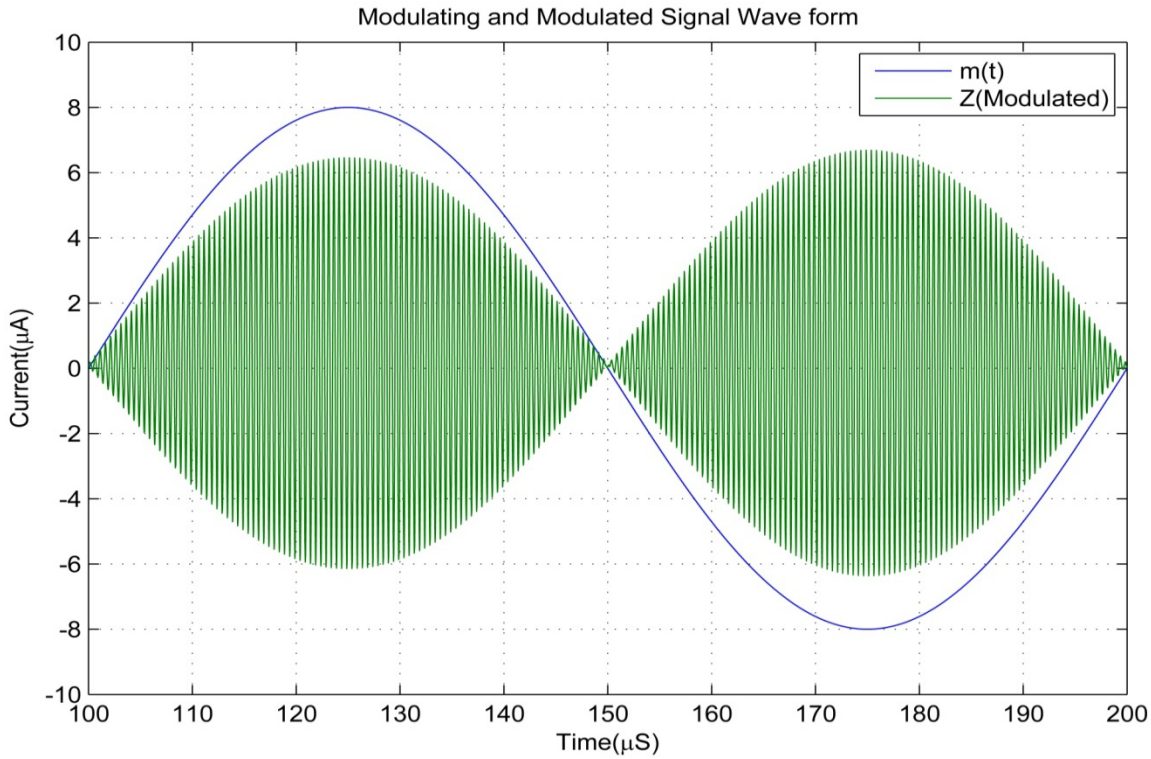


Figure 4.11 Waveform of the resulting modulated signal (z)

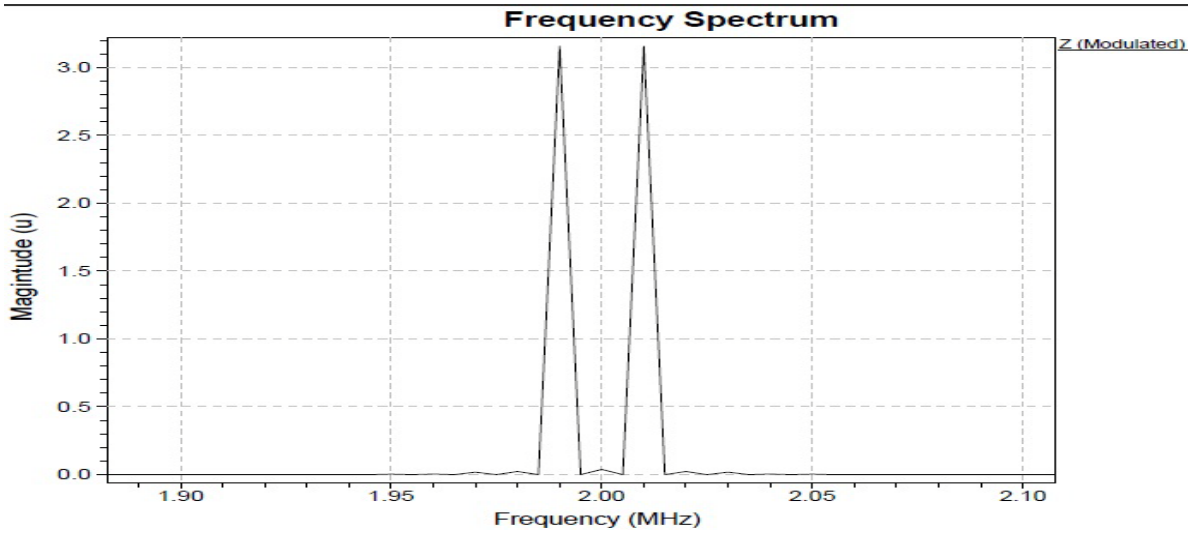


Figure 4.12 Frequency spectrum of modulated Signal (z)

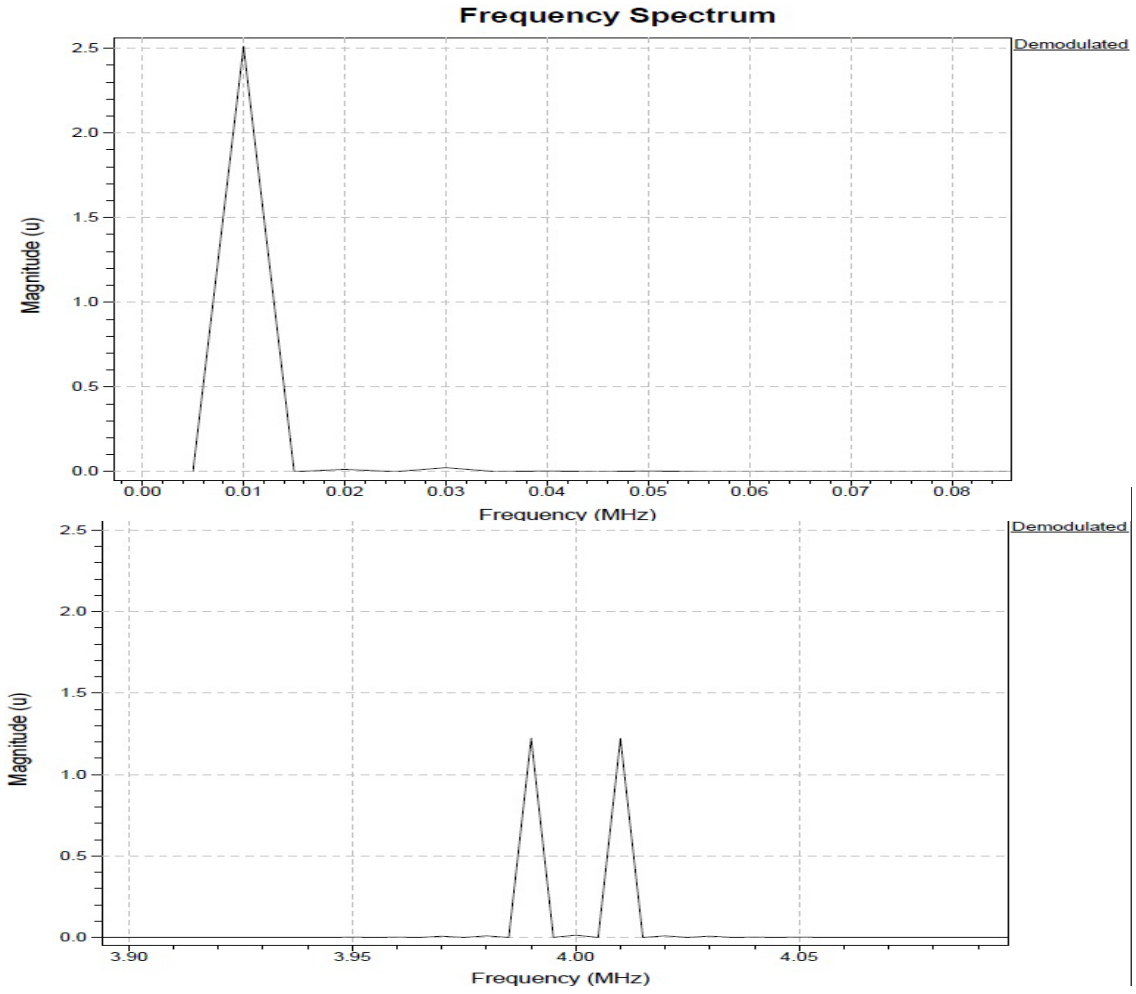


Figure 4.13 Frequency spectrum of demodulated signal before filtering

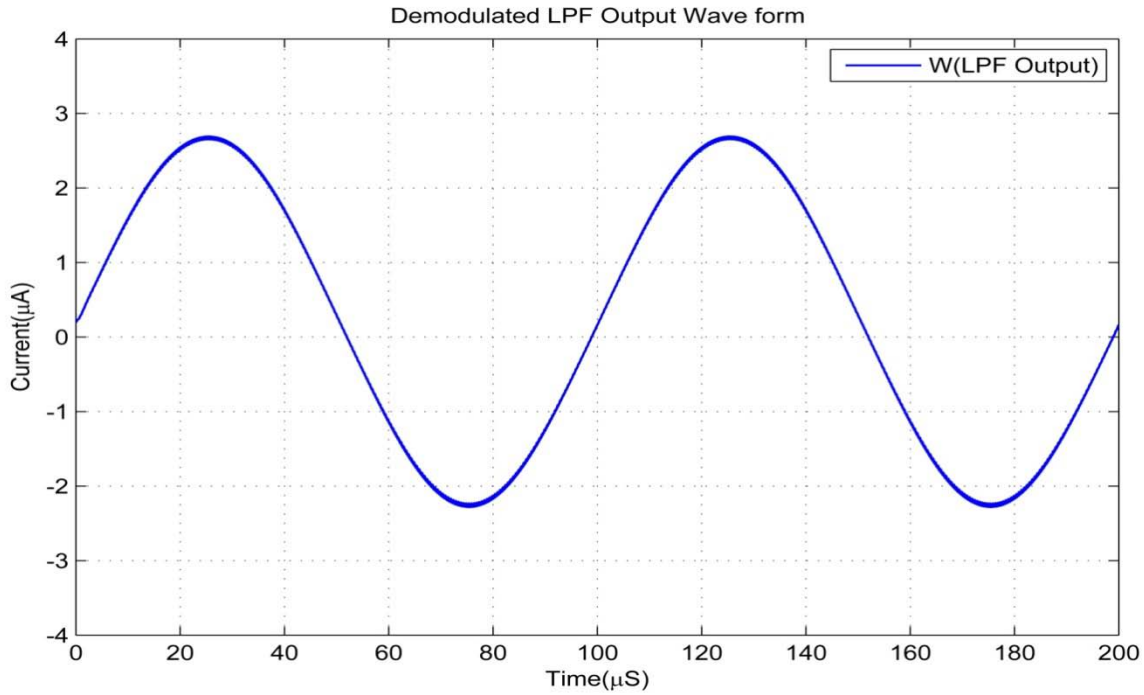


Figure 4.14 Waveform of reconstructed output signal after LPF (w)

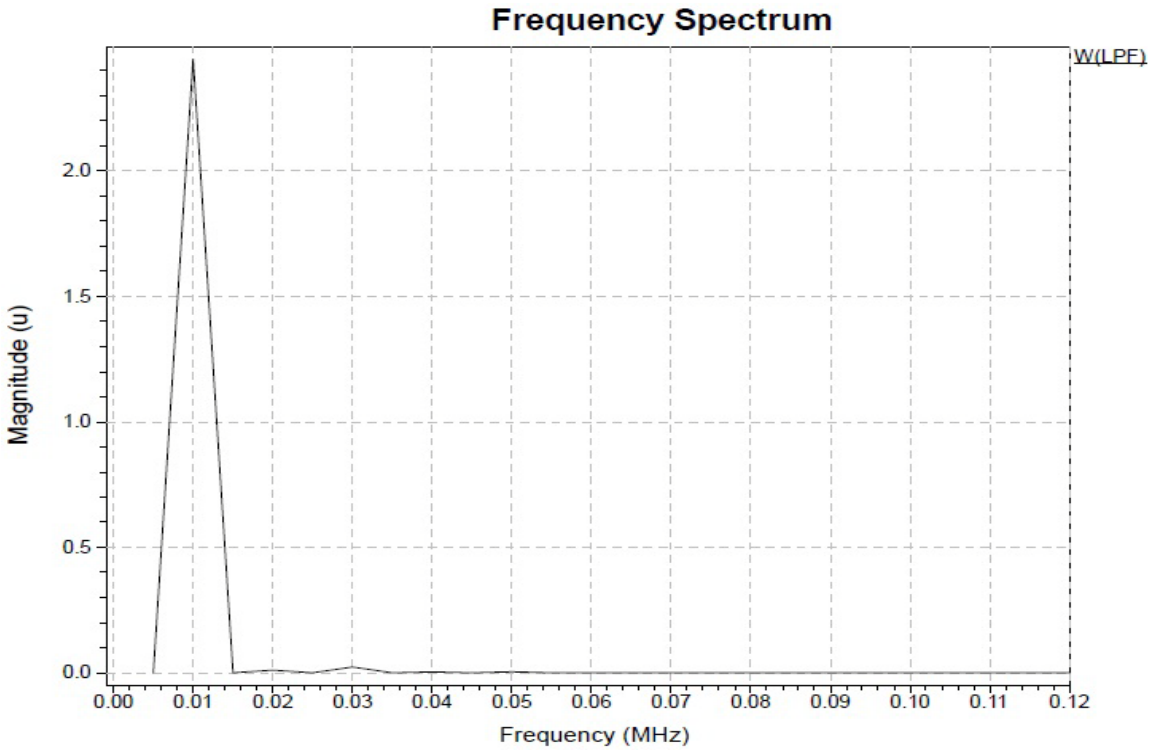


Figure 4.15 Frequency spectrum of reconstructed output signal after LPF (w)

4.4 Phase Detector

The phase detector is an essential block of the phase locked loop system. In this application, three CAB units are used to realize a phase detector which could be used in PLL. Figure (4.16) shows the block diagram of the CABs used in the phase detector. In the figure, CAB_1 is configured as a multiplier while $CAB_2\ and\ CAB_3$ are used to realize a LPF. This LPF is the same one used previously in modulation-demodulation system application in figure (4.9). The idea behind the phase detector design is to generate a signal that is proportional to the phase difference of the two input signals. The multiplier does generate this signal and the LPF removes the unwanted components [49, 61 and 62]. In figure (4.16), assuming the two inputs are:

$$m_1(t) = A_1\sin(\omega t + \theta_1) \tag{4.27}$$

$$m_2(t) = A_2\cos(\omega t + \theta_2) \tag{4.28}$$

Then, z which is the output of the multiplier (CAB_1) can bewritten as:

$$z = \frac{m_1(t)*m_2(t)}{I_b} = \frac{A_1A_2}{2*I_b}[\sin(2\omega t + \theta_1 + \theta_2) + \sin(\theta_1 - \theta_2)] \tag{4.29}$$

It is clear from equation (4.29) that the first term is a high frequency component and the second term is a low frequency component. If a LPF is used the second term will be retained. This term is a function of the phase difference between the two input signals $m_1(t) and\ m_2(t)$. Therefore the output of the LPF (w)will be:

$$w = \frac{A_1A_2}{2*I_b}[\sin(\theta_1 - \theta_2)] \tag{4.30}$$

The following values are selected in order to test the proposed phase detector:

The amplitude of the two input signals $A_1 = A_2 = 8\mu A$, frequency $\frac{\omega}{2\pi} = 2MHz$, phase $\theta_2 = 0\ and\ \theta_1$ is swept from $0°\ to\ 360°$.

Figure (4.17) shows the transfer characteristic of the phase detector $(w\ versus\ \theta_d)$ where θ_d represent the phase difference $(\theta_1 - \theta_2)$ and w is produced in response to this difference. It can be noticed from this figure that the characteristic is a sinusoidal like wave repeating every $360°$ as suggested by equation (4.30). However, there is a small error in the response about $3°$, which is mainly due to the phase shift error from the CAB due to the accumulation of parasitic capacitance in all stages.

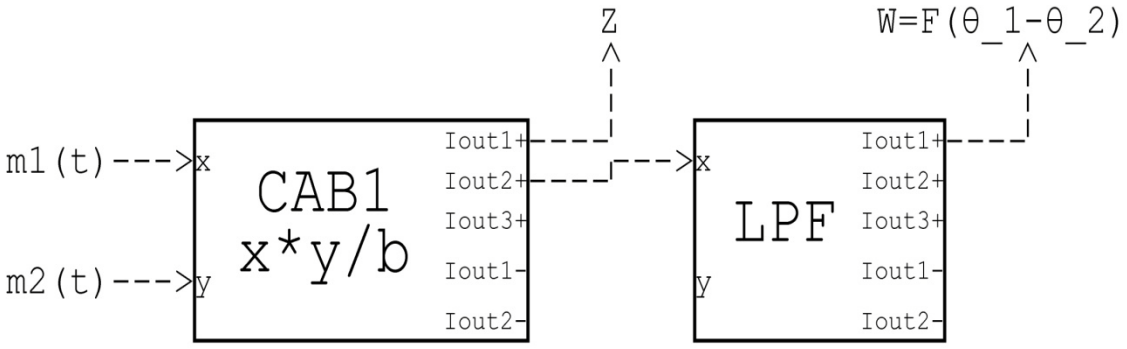


Figure 4.16 Phase detector block diagram, the LPF is shown in figure (4.10)

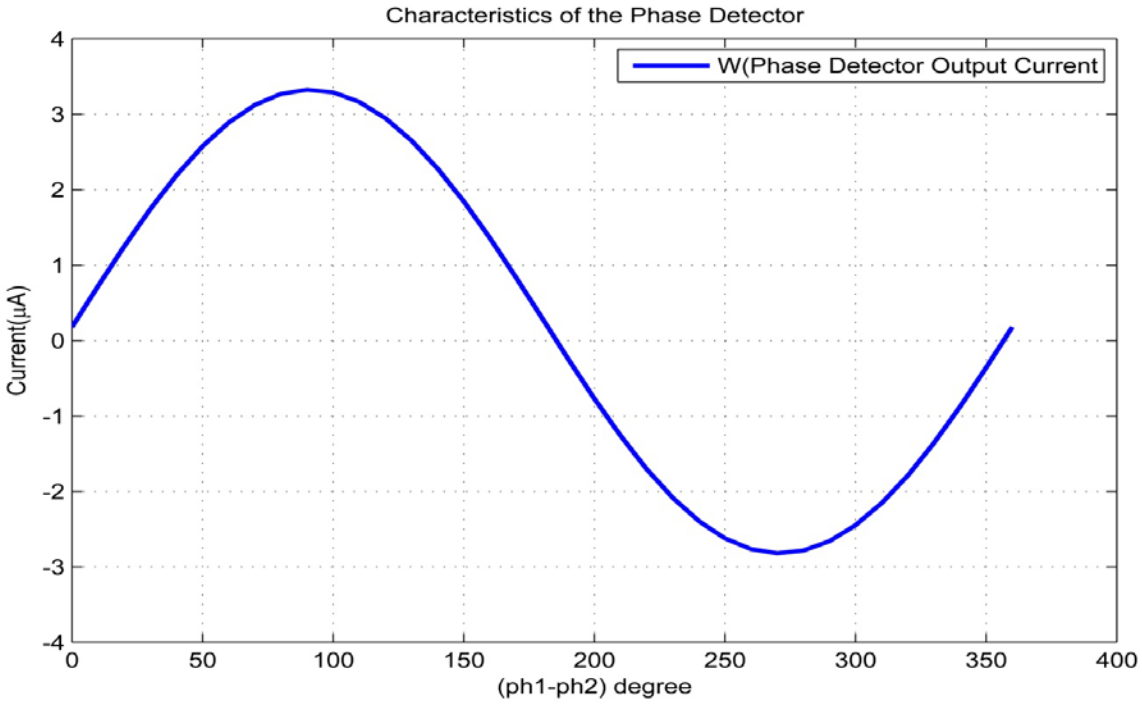


Figure 4.17 Phase detector characteristic (output current (w) VS phase difference)

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, the design of configurable analog block (CAB) for field programmable analog array (FPAA) has been presented. This design is based on current mode MOSFET transistor level operating in saturation region. The design of three functional cells which are: addition-subtraction, integration and multiplication/division cell has been developed. Moreover, the programming and tuning of the CAB is achieved through altering the circuits biasing condition in addition to some switches. In order to confirm the proper functionality as well as the validity of the proposed CAB, it has been utilized to realize different applications using more than one unit in each structure. These realized application structures are:

- A universal second order filter
- A fourth order band pass filter
- A modulation/demodulation system.
- A phase detector

The proposed design in this work has proven its validity and feasibility through its use in designing different applications. In addition, there is a lack of designs in the literature adopting the method used in this work which gives an advantage to this proposed design.

The main attractive features of this design over some previous designs are small size, simplicity, low power consumption and high bandwidth.

This is considered to be as a part of the ongoing improvements in the field of configurable analog blocks. The results of this work in collaboration with previous research in this field will be very useful for other researchers and other interested people in the same area.

5.2 Future Work

The following point can be part of the improvement of this work since there is always a room for improvement:

- Improving the proposed multiplier/divider in order to have better division functionality by not making the divider the same as the bias current.
- Adding the capability of the control over the quality factor (Q) in the filter design.
- Improving the supplementary and biasing circuits used in order to enhance the CAB bandwidth and reduce the linearity error and phase shift errors.
- Adding extra functions such as exponential and differential in order to widen its area of application.
- Extending the application area of the Cab such as building a universal filter realized to a higher order system.
- The feature size of the technology used to design the CAB can be smaller than $0.35\mu m$ process used by which it will be allowed to interface more easily with recent digital technology and consume less area.

- Producing the layout of the proposed CAB and doing post-layout simulation.
- Fabrication of the proposed CAB and experimentally testing its validity in order to compare it with the theory and simulation results.

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